

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		625211	PRODUCTION RELEASED	08/29/08	?

# M97 MLB SCHEMATIC

REFERENCED FROM T18  
08/27/2008

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33	Ethernet PHY (RTL8211CL)	SUMA	05/23/2008
34	Ethernet & AirPort Support	SUMA	07/01/2008
35	ETHERNET CONNECTOR	SUMA	04/04/2009










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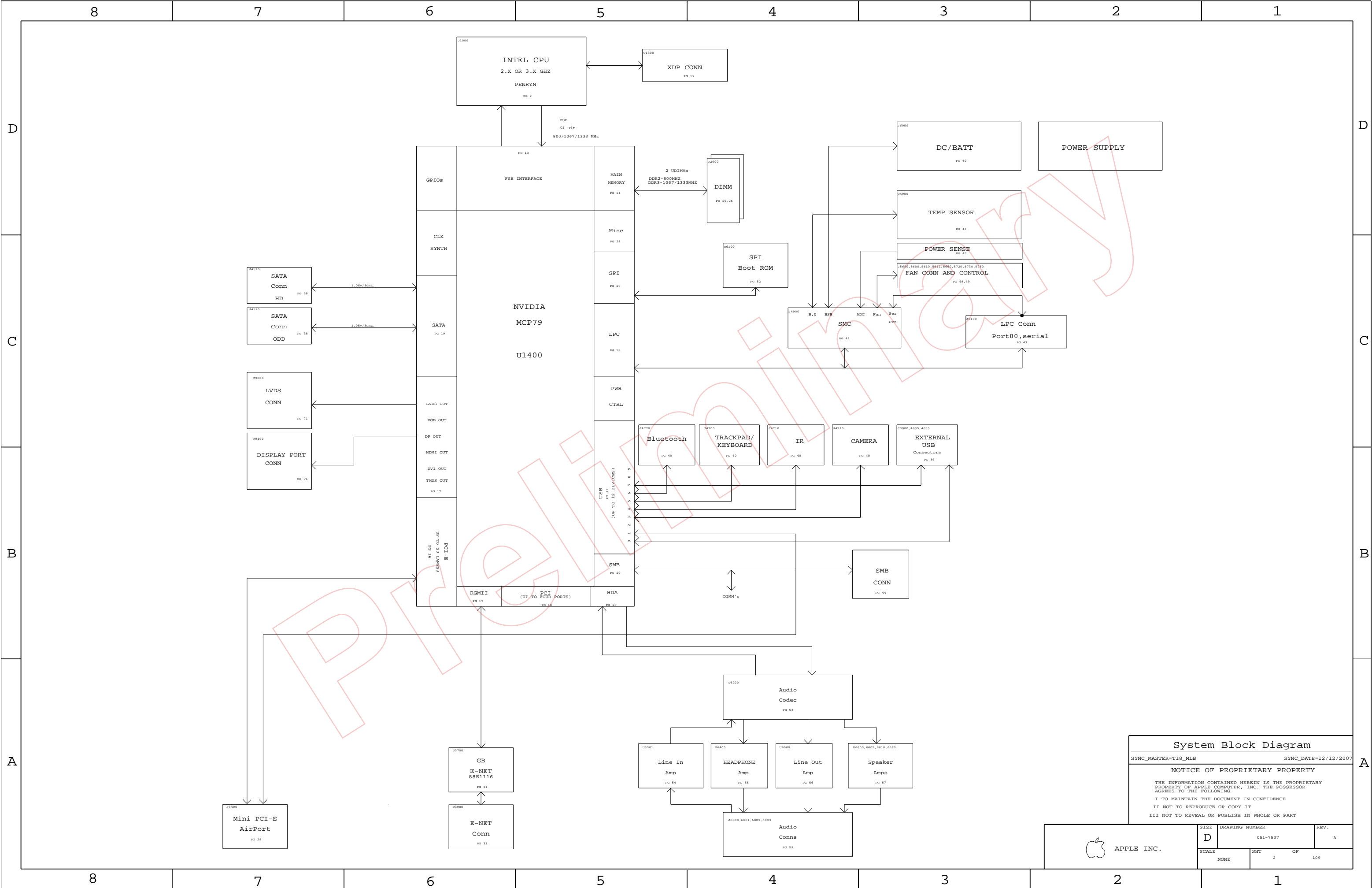
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# PVT BUILD

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7537	1	SCHEM,MLB,M97	SCH	CRITICAL	
820-2327	1	PCBF,MLB,M97	PCB	CRITICAL	

<p>DIMENSIONS ARE IN MILLIMETERS</p> <p>XX ± _____</p> <p>X.XX ± _____</p> <p>X.XXX ± _____</p> <p>ANGLES ± _____</p> <p>DO NOT SCALE DRAWING</p>	<p>METRIC</p>				<p> APPLE INC.</p>			
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	<p>DRAFTER</p>		<p>DESIGN CK</p>		<p>TITLE</p> <p>SCHEM,MLB,M97</p>			
	<p>ENG APPD</p>		<p>MFG APPD</p>					
<p>QA APPD</p>		<p>DESIGNER</p>						
<p></p> <p>THIRD ANGLE PROJECTION</p>	<p>RELEASE</p>		<p>SCALE</p> <p>NONE</p>					
	<p>MATERIAL/FINISH</p> <p>NOTED AS</p> <p>APPLICABLE</p>		<p>SIZE</p> <p>D</p>		<p>DRAWING NUMBER</p> <p>051-7537</p>		<p>REV.</p> <p>A</p>	
					<p>SHEET 1 OF 109</p>			



System Block Diagram

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=12/12/2007

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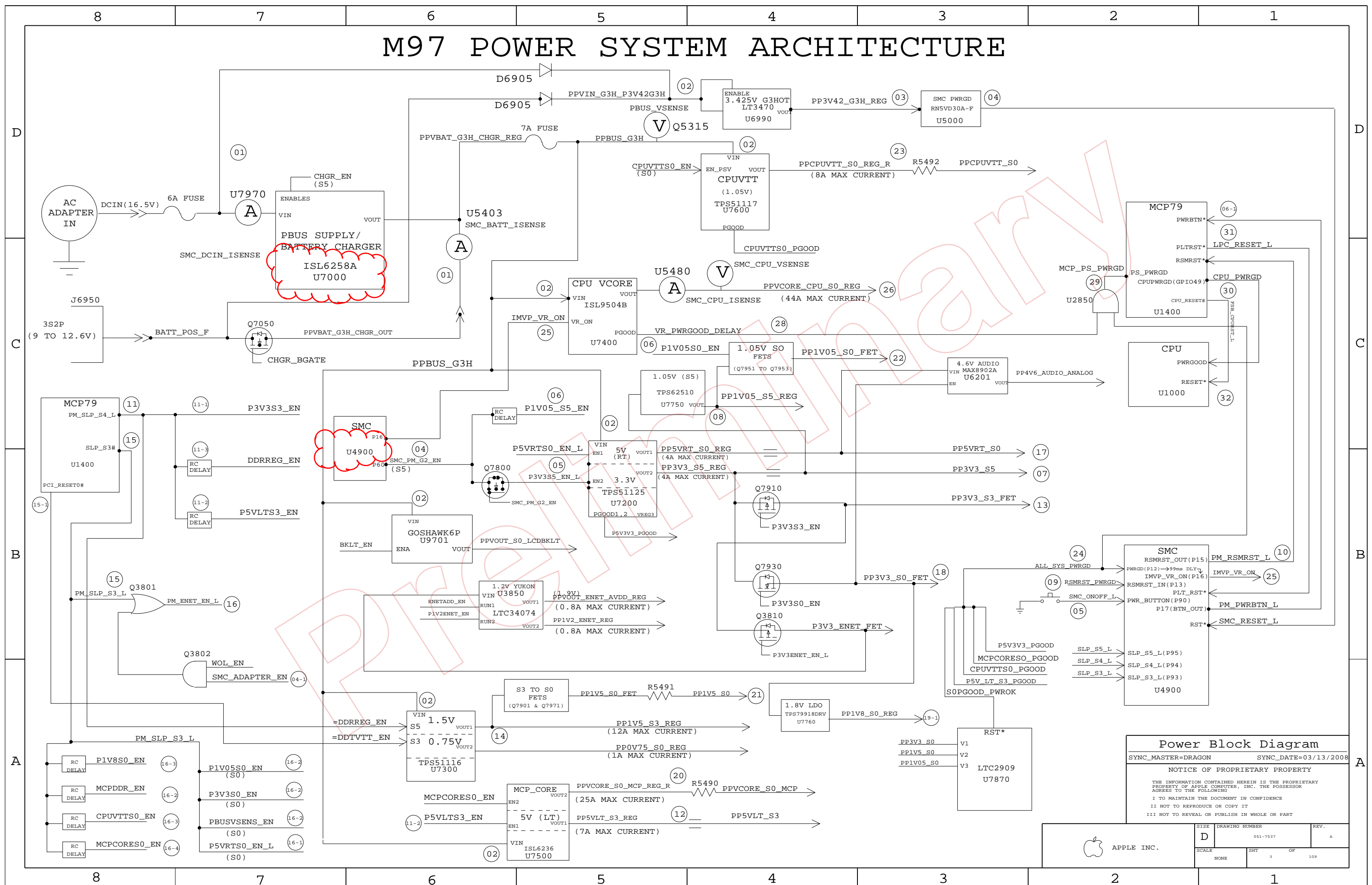
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# M97 POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9554	PCBA, MLB, BETTER, M97	M97_COMMON, CPU_2_0GHZ, EEE_2KA
630-9314	PCBA, MLB, BEST, M97	M97_COMMON, CPU_2_4GHZ, EEE_1DJ

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2K9]	CRITICAL	EEE_2K9
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2KA]	CRITICAL	EEE_2KA
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:1DJ]	CRITICAL	EEE_1DJ

BOM Groups

BOM GROUP	BOM OPTIONS
M97_COMMON	COMMON, ALTERNATE, M97_MCP, M97_MISC, M97_DEBUG_PVT, M97_PROGPARTS
M97_MCP	MCP_B02, MCP_PROD, MEMRESET_HW, MEMRESET_MCP, BOOT_MODE_USER, MCPSEQ_SMC, MCP_CS1_NO
M97_MISC	ONEWIRE_PU, BKLT_PLL_NOT, DP_ESD, ENG_BMON, MIKEY
M97_PROGPARTS	BOOTROM_PROG, SMC_PROG, IR_PROG, WELLSPRING_PROG
M97_DEBUG_ENG	SMC_DEBUG_YES, XDP, XDP_CONN, LPCPLUS, VREFMRGN, TPAD_DEBUG
M97_DEBUG_PVT	SMC_DEBUG_YES, XDP, LPCPLUS, NO_VREFMRGN
M97_DEBUG_PROD	SMC_DEBUG_YES, XDP, LPCPLUS_NOT, NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3622	1	PDC, QJGL, QS, 2.0, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_2_0GHZ_QS
337S3624	1	PDC, QDYD, QS, 2.26, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_2_26GHZ_QS
337S3625	1	PDC, QDVJ, QS, 2.4, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ_QS
337S3646	1	PDC, SLOBE, PRQ, 2.0, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3653	1	PDC, SL3BU, PRQ, 2.26, 25W, 1066, CO, 3M, BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC, SLB4N, PRQ, 2.4, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0540	1	IC, GMCP, MCP79, 35X35MM, BGA1437, A01	U1400	CRITICAL	MCP_A01
338S0591	1	IC, GMCP, MCP79, 35X35MM, BGA1437, A01P	U1400	CRITICAL	MCP_A01P
338S0603	1	IC, GMCP, MCP79, 35X35MM, BGA1437, A01Q	U1400	CRITICAL	MCP_A01Q
338S0600	1	IC, GMCP, MCP79, 35X35MM, BGA1437, B01	U1400	CRITICAL	MCP_B01
338S0635	1	IC, GMCP, MCP79, 35X35MM, BGA1437, B02	U1400	CRITICAL	MCP_B02
338S0570	1	IC, RTL8211CL, GIGE TRANSCEIVER, 48P, TQFP	U3700	CRITICAL	

Programmable Parts

338S0563	1	IC, SMC, MS8/2117, 9X9MM, TLP, HP	U4900	CRITICAL	SMC_BLANK
341S2287	1	IC, SMC, M97	U4900	CRITICAL	SMC_PROG
335S0610	1	IC, FLASH, SP1, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2285	1	IC, PRGRM, EP1 BOOTROM, UNLOCK, M97	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC, CY7C63833, ENCORE II, USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC, IR CONTROLLER, M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC, PSOC+ W/ USB, 56 PIN, MLP, CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2348	1	IC, WELLSPRING CONTROLLER, M97	U5701	CRITICAL	WELLSPRING_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
514-0612	514-0607		ALL	FOXLINK AS ALTERNATE
514-0613	514-0608		ALL	FOXLINK AS ALTERNATE

M97 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

BOM Configuration

SYNC\_MASTER=M97\_MLB

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SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7537

SHT

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REV.

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OF

109

APPLE INC.

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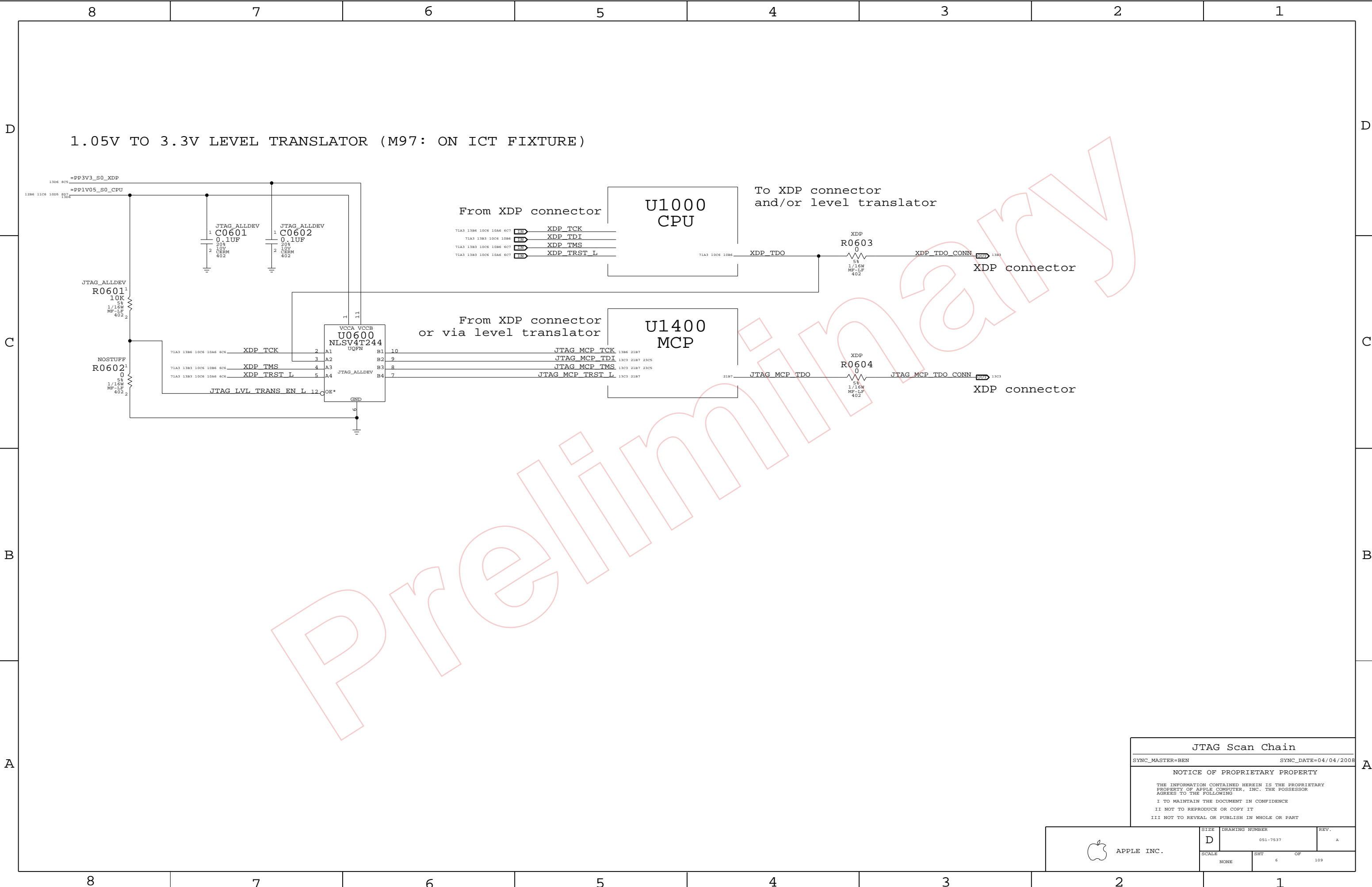
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C							C
B							B
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Preliminary

Revision History

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REV.	A	

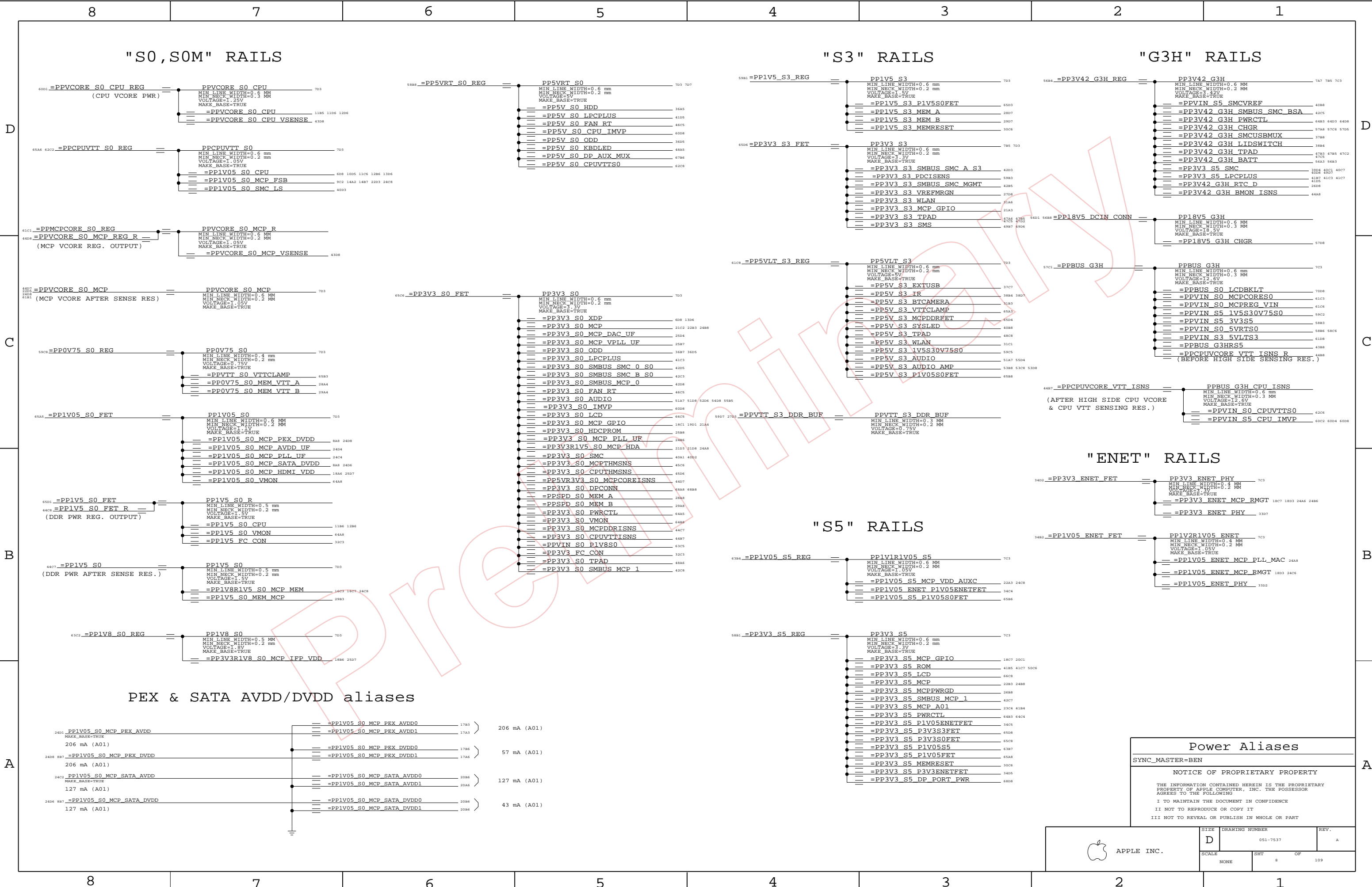
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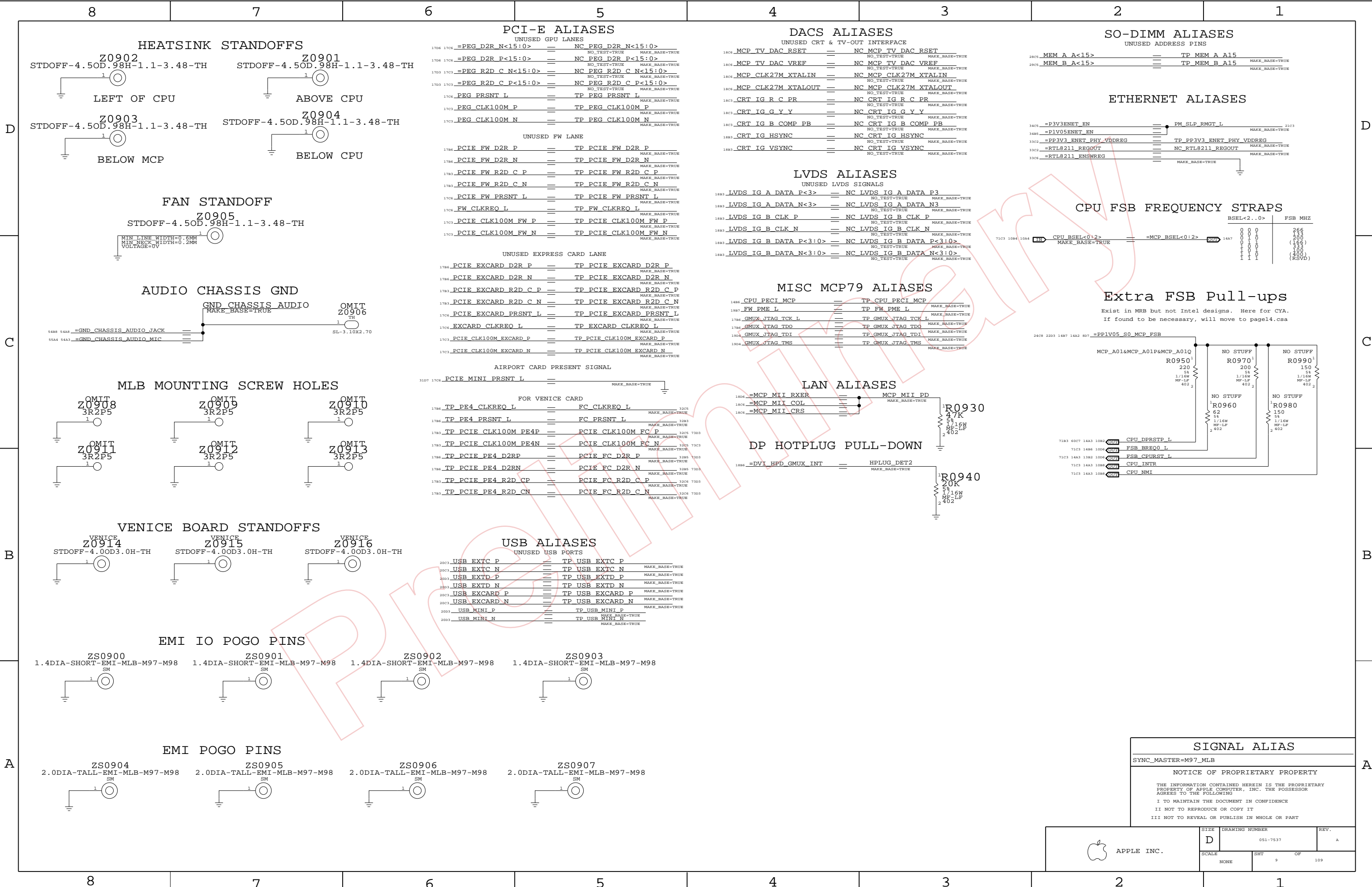
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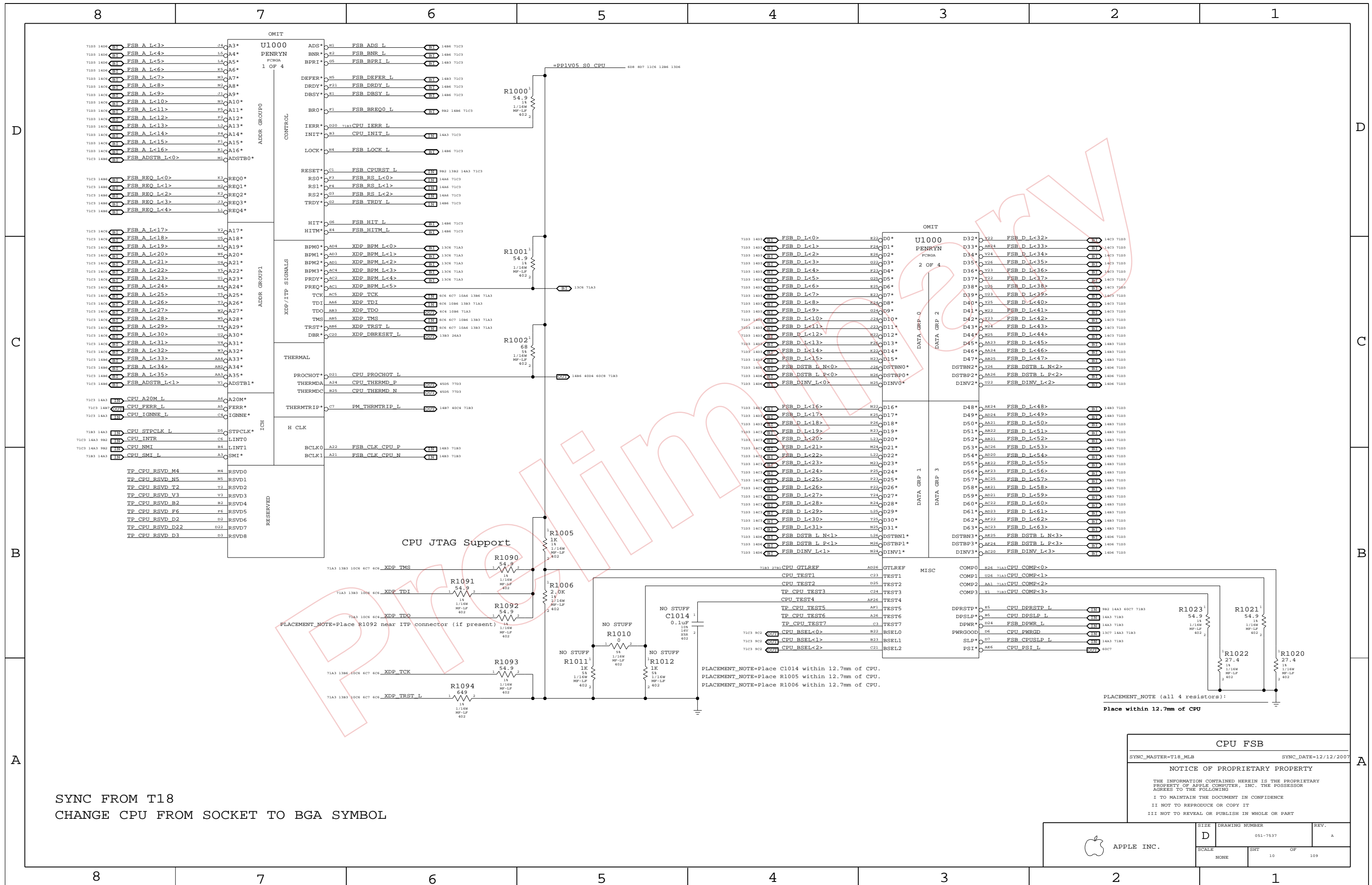


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Functional Test Points							
D	Fan Connectors		RIGHT CLUTCH CONN		DEBUG VOLTAGE		
	1800	TRUE PP5VRT S0 (NEED 3 TP) 703 805	1800	TRUE PP5V S3 BTCAMERA F 3187	1800	TRUE PPVCORE S0 CPU 807	
	1801	TRUE FAN RT PWM 4684	1801	TRUE PCIE MINI D2R P 1786 3107 7303	1801	TRUE PPCPUVTT S0 807	
	1802	TRUE FAN RT TACH 4604	1802	TRUE PCIE MINI D2R N 1786 3107 7303	1802	TRUE PPVCORE S0 MCP 807	
		(NEED TO ADD 3 GND TP)	1803	TRUE PCIE MINI R2D P 3107 7303	1803	TRUE PP0V75 S0 807	
	MIC FUNC_TEST		1804	TRUE PCIE MINI R2D N 3107 7303	1804	TRUE PP1V05 S0 807	
	1805	TRUE MIC HI CONN 5481 5402	1805	TRUE PCIE CLK100M MINI CONN P 3108 7303	1805	TRUE PP1V5 S0 887	
	1806	TRUE MIC LO CONN 5481 5402	1806	TRUE PCIE CLK100M MINI CONN N 3108 7303	1806	TRUE PP1V8 S0 887	
	1807	TRUE MIC SHLD CONN 5402 55A6	1807	TRUE USB CAMERA CONN P 3187 7403	1807	TRUE PP5VRT S0 707 805	
			1808	TRUE USB CAMERA CONN N 3187 7403	1808	TRUE PP3V3 S0 805	
C	SPEAKER FUNC_TEST		1809	TRUE PP5V WLAN 703 3105	1809	TRUE PP1V5 S3 803	
	1809	TRUE SPKRAMP L N OUT 53A2 54C2	1810	TRUE PCIE WAKE L 1786 2305 3107	1810	TRUE PP3V3 S3 785 803	
	1810	TRUE SPKRAMP L P OUT 53B2 54C2	1811	TRUE SMBUS SMC A S3_SCL 785 4202 76D3	1811	TRUE PP5VLT S3 803	
	1811	TRUE SPKRAMP R N OUT 53C3 54C2	1812	TRUE SMBUS SMC A S3_SDA 785 4202 76D3	1812	TRUE PP1V1R1V05 S5 883	
	1812	TRUE SPKRAMP R P OUT 53C3 54C2	1813	TRUE CONN USB2 BT P 3187 7483	1813	TRUE PP3V3 S5 883	
	1813	TRUE SPKRAMP SUB N OUT 53B2 54C2	1814	TRUE CONN USB2 BT N 3187 7483	1814	TRUE PP3V42 G3H 7A7 785 8D1	
	1814	TRUE SPKRAMP SUB P OUT 53B2 54C2	1815	TRUE MINI CLKREQ O L 3107	1815	TRUE PPBUS G3H 801	
			1816	TRUE MINI RESET CONN L 31A7	1816	TRUE PP3V3 ENET PHY 881	
				(NEED TO ADD 3 GND TP)	1817	TRUE PP1V2R1V05 ENET 881	
			SATA HDD CONN (NEED 4 TP)		1818	TRUE PP3V3 G3_RTC 2108 22A5 26D4	
B	THERMAL FUNC_TEST		1818	TRUE PP5V S0 HDD_FLT 703 36A7	1818	TRUE PP5V WLAN 705 3105	
	1818	TRUE MCPTHMSNS D2_P 45B5 77D3	1819	TRUE SATA HDD R2D P 36A7 73A3	1819	TRUE PP5V SW_ODD 787 36D3	
	1819	TRUE MCPTHMSNS D2_N 45B5 77D3	1820	TRUE SATA HDD R2D N 36A7 73A3	1820	TRUE PP5V S0 HDD_FLT 705 36A7	
	LVDS FUNC_TEST		1821	TRUE SATA HDD D2R C_P 36A7 73A3	1821	TRUE PP3V3 S5_AVREF_SMC 39D4 40B6	
	1820	TRUE PP3V3 LCDVDD_SW_F 703 66C2	1822	TRUE SATA HDD D2R C_N 36A7 73A3	1822	TRUE PP18V5 S3 705 48C1 48D3	
	1821	TRUE PP3V3 S0_LCD_F 66C3	1823	TRUE SATA ODD_R2D_N 787 36B5 73A3	1823	TRUE PP3V3 S3_LDO 707 66C2	
	1822	TRUE PPVOUT S0_LCDBKLT 703 66B2 69B3 69C1		(NEED TO ADD 4 GND TP)	1824	TRUE PP3V3 LCDVDD_SW_F 69A8 69B6 69C4 69C8	
	1823	TRUE LVDS_IG_DDC_CLK 38A3 66C5	IPD_FLEX_CONN		1825	TRUE PPVOUT S0_LCDBKLT 51A3 51D3 52D6	
	1824	TRUE LVDS_IG_DDC_DATA 38A3 66B5	1824	TRUE PP3V3 S3_LDO 703 48B4 48C3	1826	TRUE TRUE SMC_PM_G2_EN 39D5 64D8	
	1825	TRUE LVDS_IG_A_DATA_N<0> 1883 66C2 73B3	1825	TRUE PP18V5 S3 703 48C1 48D3	1827	TRUE PM_SLP_S4_L 21C3 39C5 40A2 64C8	
A	1826	TRUE LVDS_IG_A_DATA_P<0> 1883 66C2 73B3	1826	TRUE TPAD_GND_F 48B4 48C3 48C4 48C7	1828	TRUE PM_SLP_S3_L 21C3 34B7 39C5 41A5 64D5 68D8	
	1827	TRUE LVDS_IG_A_DATA_N<1> 1883 66C2 73B3	1827	TRUE Z2_CS_L 47C8 48C3		(NEED TO ADD 4 GND TP)	
	1828	TRUE LVDS_IG_A_DATA_P<1> 1883 66C2 73B3	1828	TRUE Z2_DEBUG3 47C8 48C3			
	1829	TRUE LVDS_IG_A_DATA_N<2> 1883 66C2 73B3	1829	TRUE Z2_MOSI 47C8 48C3			
	1830	TRUE LVDS_IG_A_DATA_P<2> 1883 66C2 73B3	1830	TRUE Z2_MISO 47C8 48C3			
	1831	TRUE LVDS_IG_A_CLK_F_N 66B2 73B3	1831	TRUE Z2_SCLK 47C8 48C3			
	1832	TRUE LVDS_IG_A_CLK_F_P 66B2 73B3	1832	TRUE Z2_BOOST_EN 48C3 48C5			
	1833	TRUE LED_RETURN_1 66B3 69C1	1833	TRUE Z2_HOST_INTN 47D8 48C3			
	1834	TRUE LED_RETURN_2 66B3 69B1	1834	TRUE Z2_BOOT_CFG1 47C8 48C3			
	1835	TRUE LED_RETURN_3 66B3 69B1	1835	TRUE Z2_CLKIN 47B6 48C3			
<div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE INC.</div></div> <div><div></div><div>APPLE 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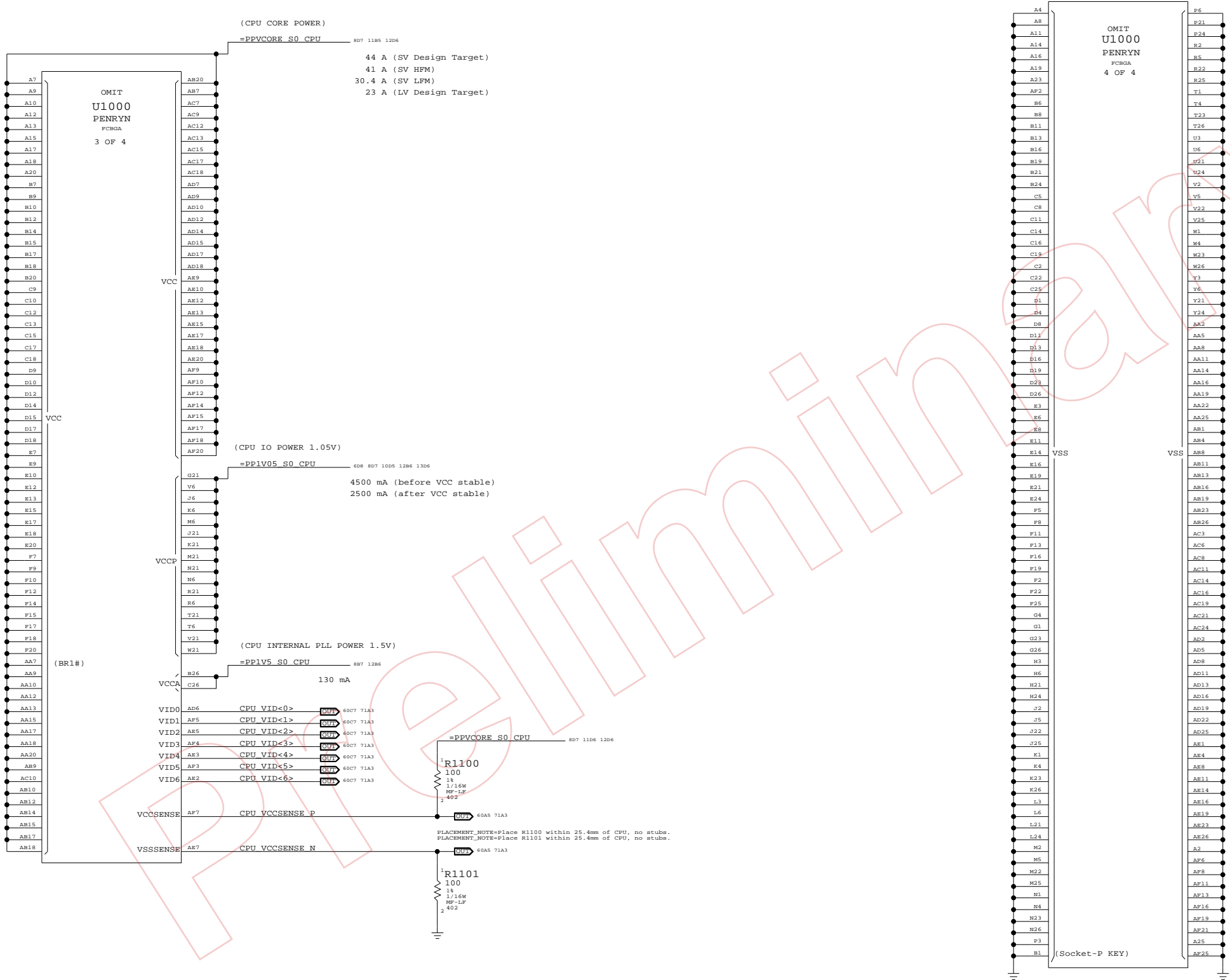
C

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A

SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.



CPU Power & Ground

SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2007

NOTICE OF PROPRIETARY PROPERTY

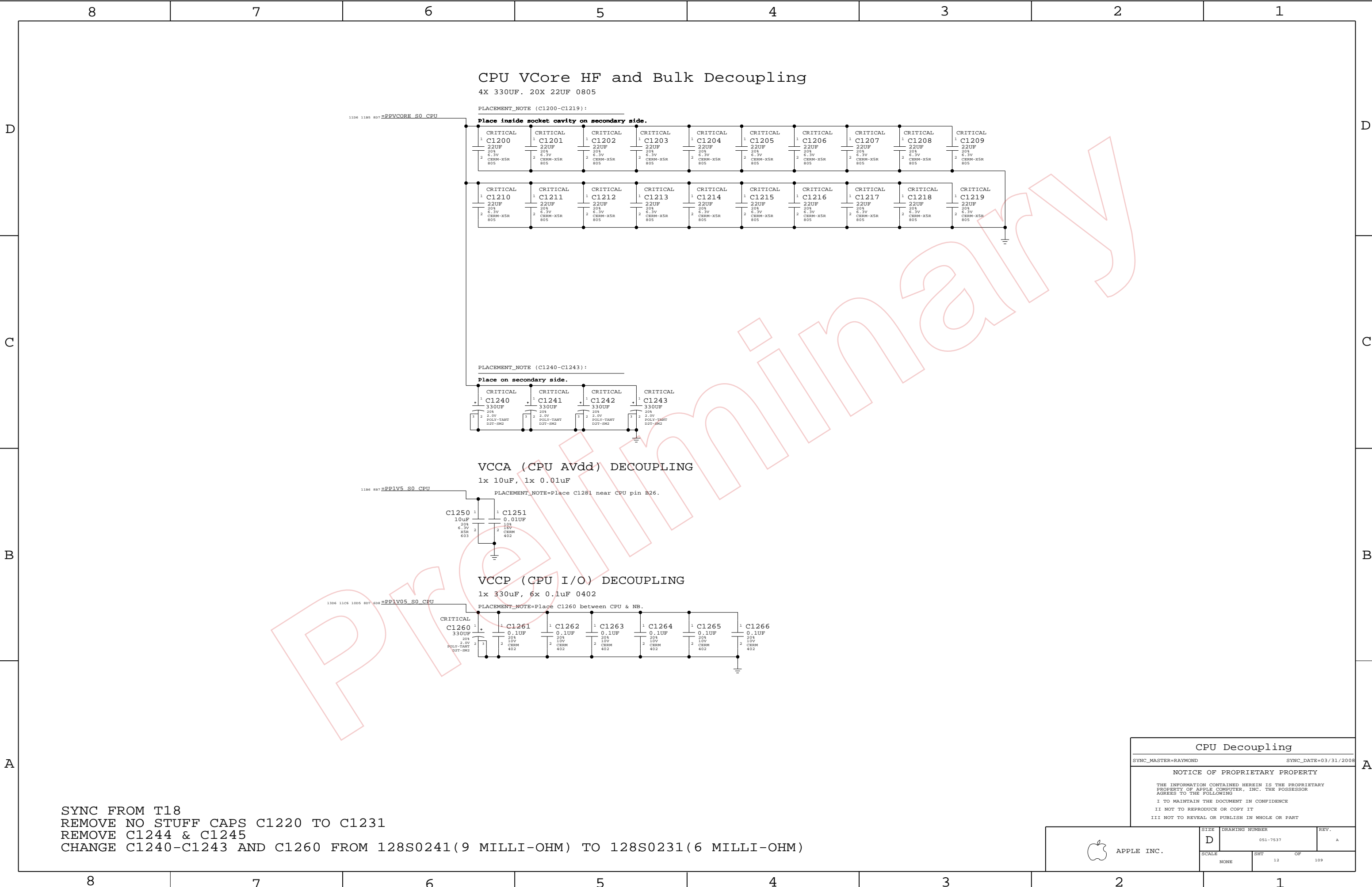
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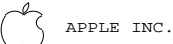
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		11	109



SYNC FROM T18  
REMOVE NO STUFF CAPS C1220 TO C1231  
REMOVE C1244 & C1245  
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

CPU Decoupling		
SYNC_MASTER=RAYMOND		SYNC_DATE=03/31/2008
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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	12	109

D

C

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A

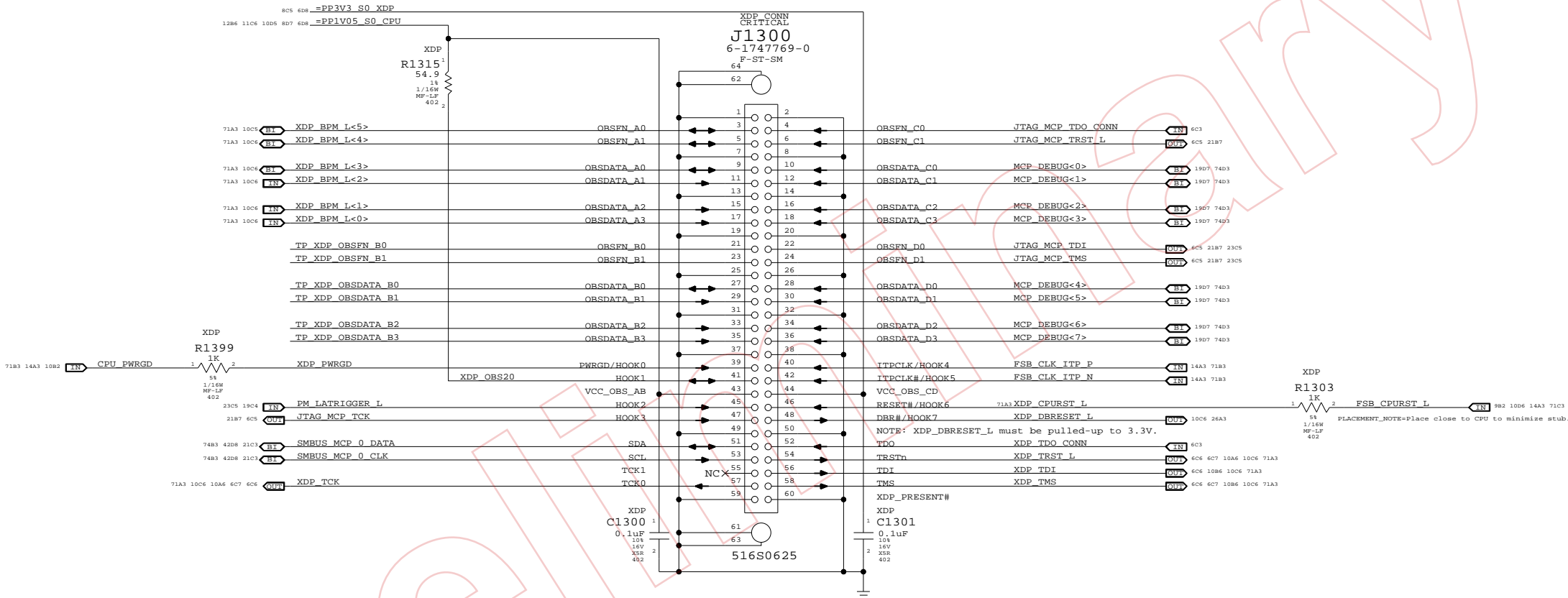
D

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A

MCP79-specific pinout

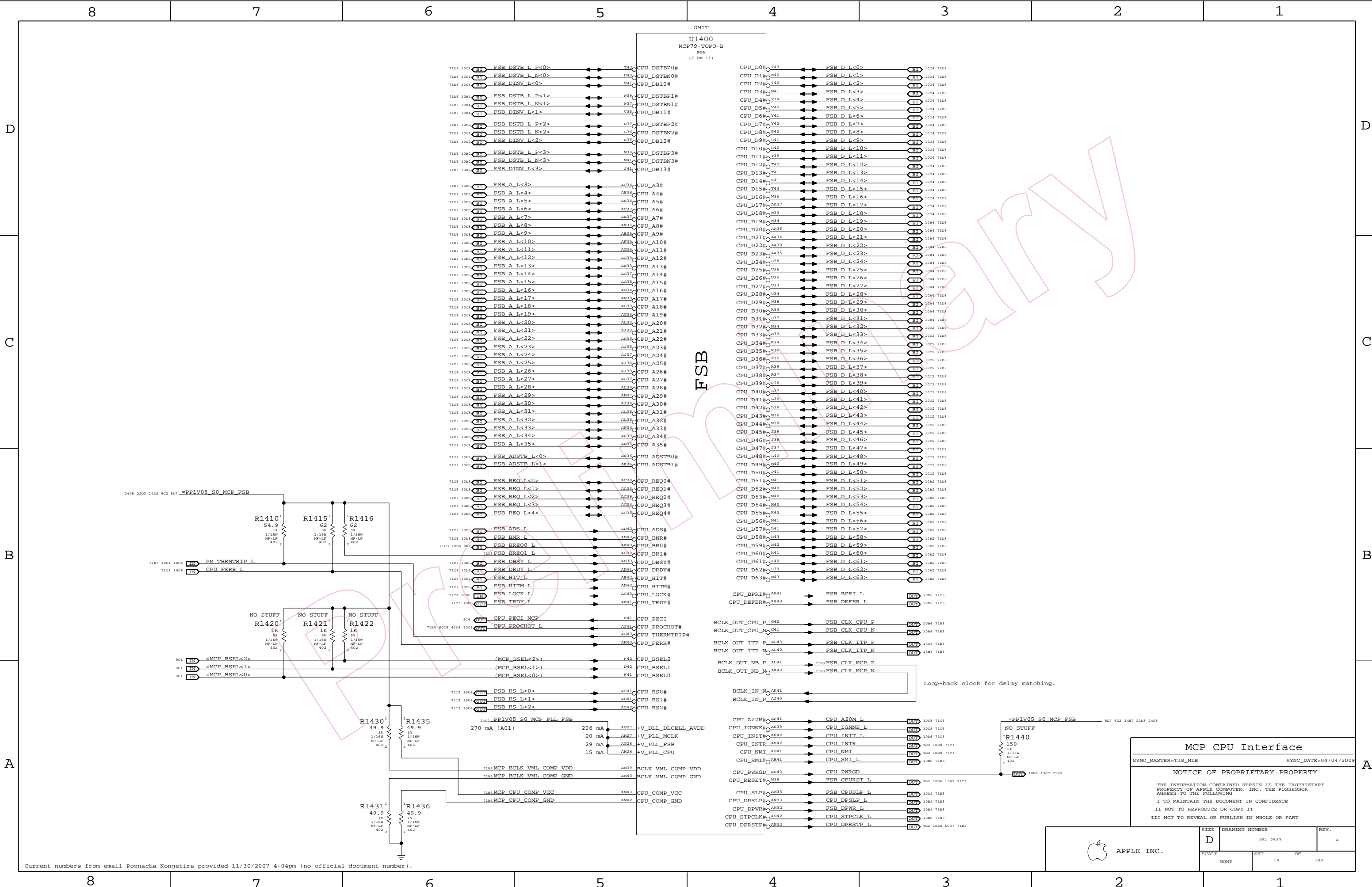


SYNC FROM T18  
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625  
RENAME JTAG\_MCP\_TDO TO JTAG\_MCP\_TDO\_CONN  
RENAME XDP\_TDO TO XDP\_TDO\_CONN

eXtended Debug Port (XDP)	
SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2007
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	D	051-7537	A
SCALE		SHT	OF
NONE		13	109

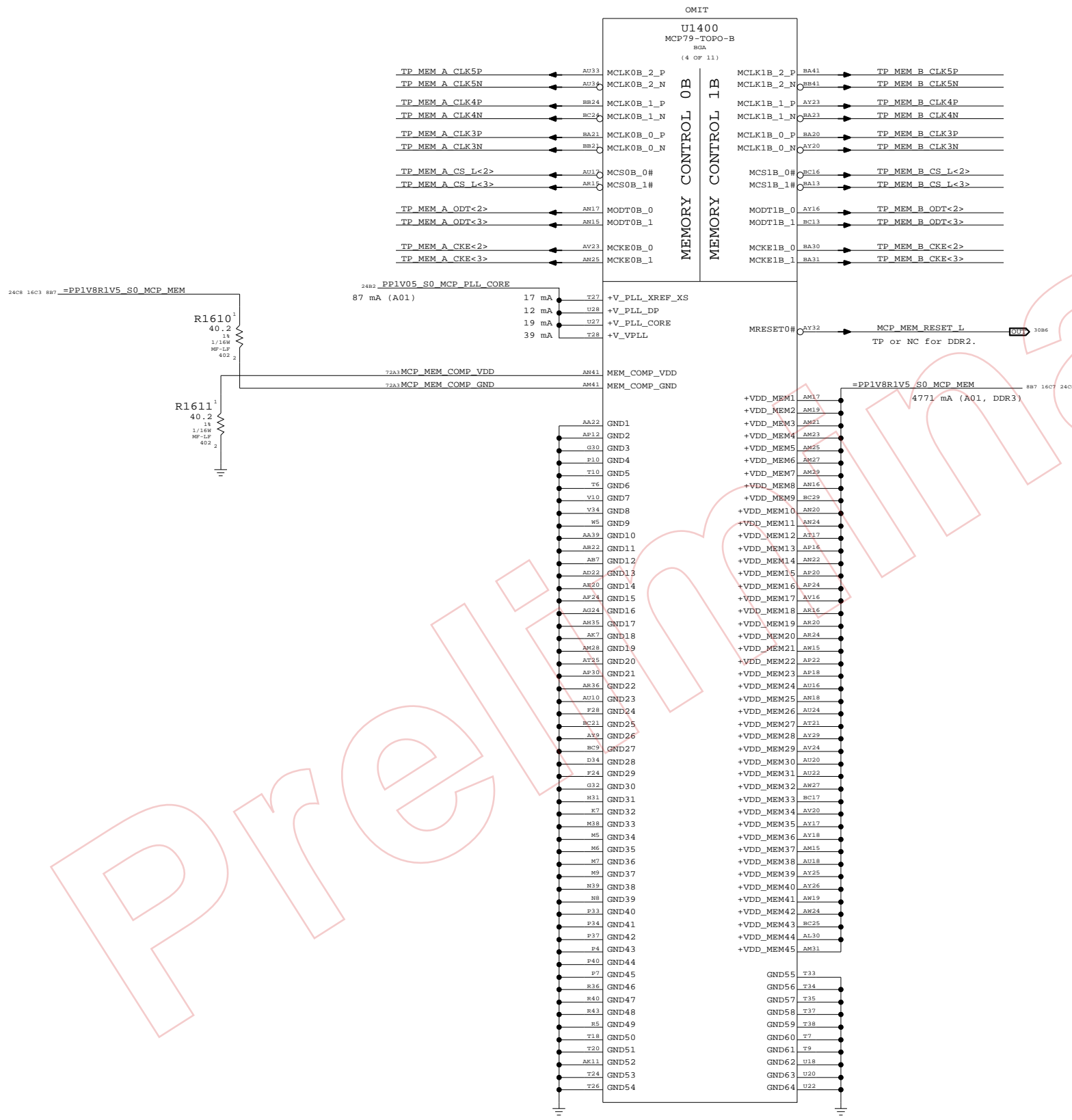







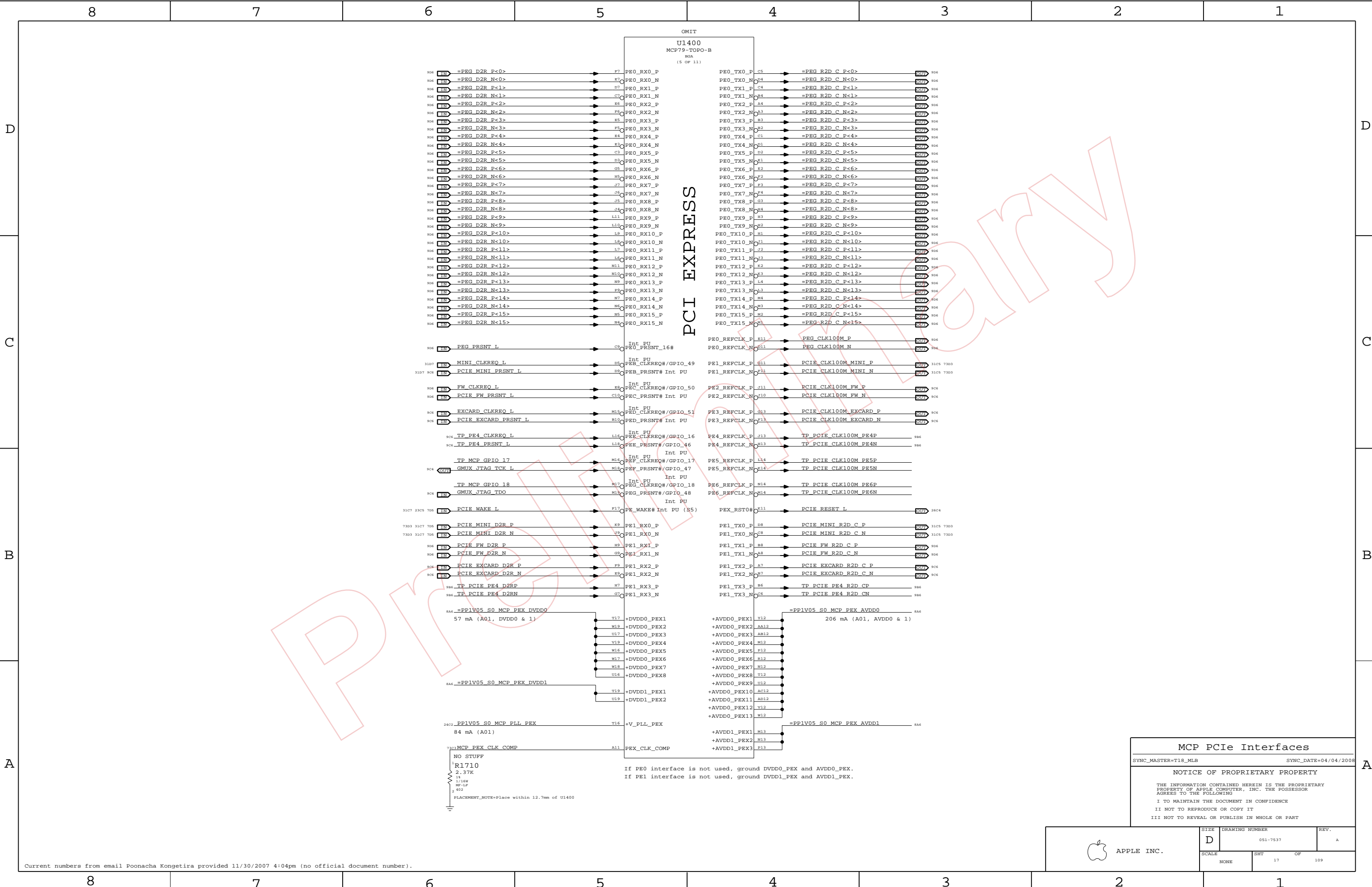
D  
  
  
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D  
  
  
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A



MCP Memory Misc	
SYNC_MASTER=T18_MLB	SYNC_DATE=04/04/2008
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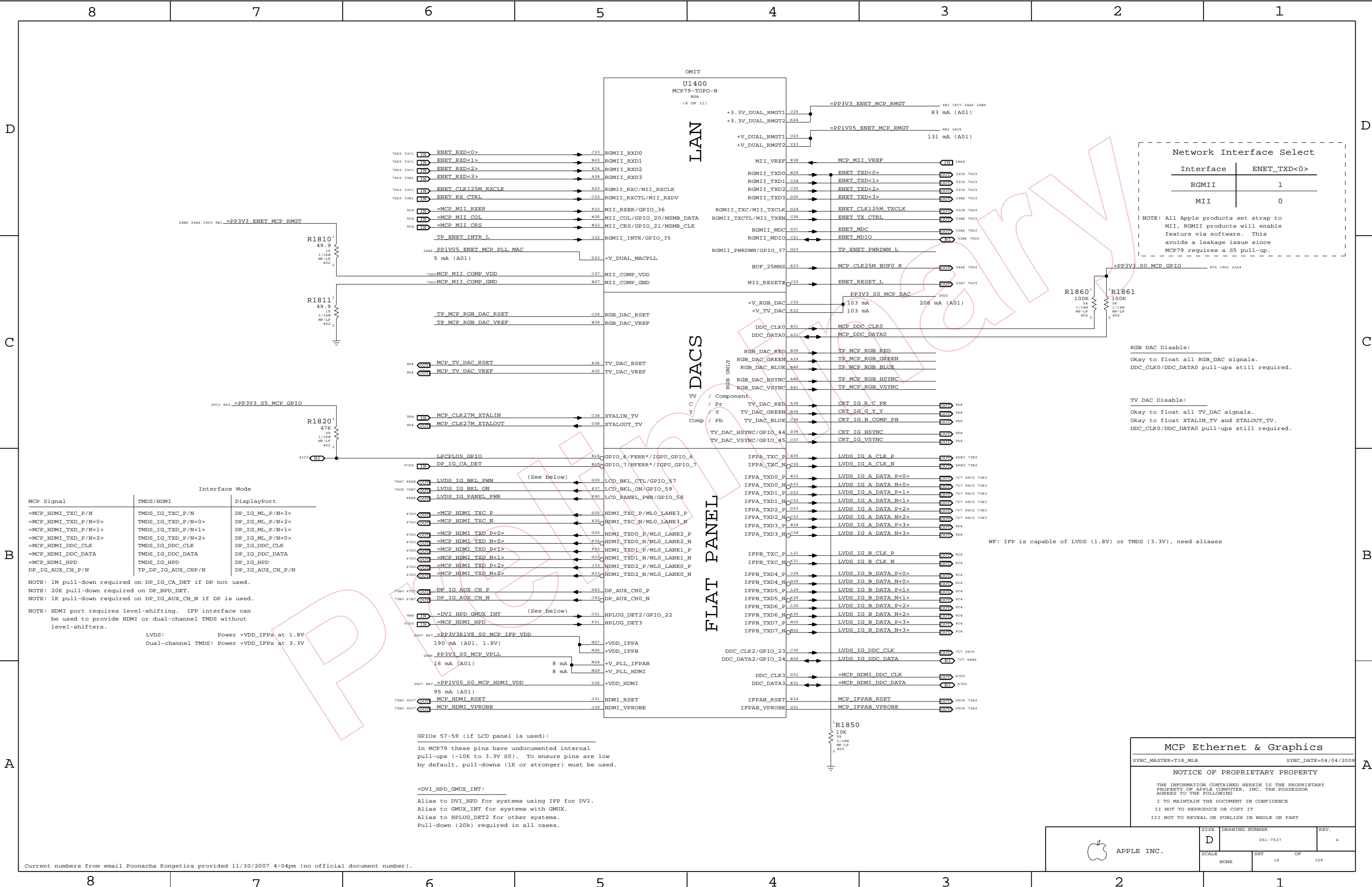
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHT 16	OF 109



MCP PCIe Interfaces		
SYNC_MASTER=T18_MLB		SYNC_DATE=04/04/2008
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	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		17	109





Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: \_\_\_\_\_  
Okay to float all RGB\_DAC signals.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required.

TV DAC Disable: \_\_\_\_\_  
Okay to float all TV\_DAC signals.  
Okay to float XTALIN\_TV and XTALOUT\_TV.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required.

Interface Mode		
MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
NOTE: 20K pull-down required on DP\_HPD\_DET.  
NOTE: 1K pull-down required on DP\_IG\_AUX\_CH\_N if DP is used.  
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD\_IPFX at 1.8V  
Dual-channel TMDS: Power +VDD\_IPFX at 3.3V

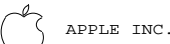
GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI\_HPD\_GMUX\_INT:

Alias to DVI\_HPD for systems using IFP for DVI.  
Alias to GMUX\_INT for systems with GMUX.  
Alias to HPLUG\_DET2 for other systems.  
Pull-down (20k) required in all cases.

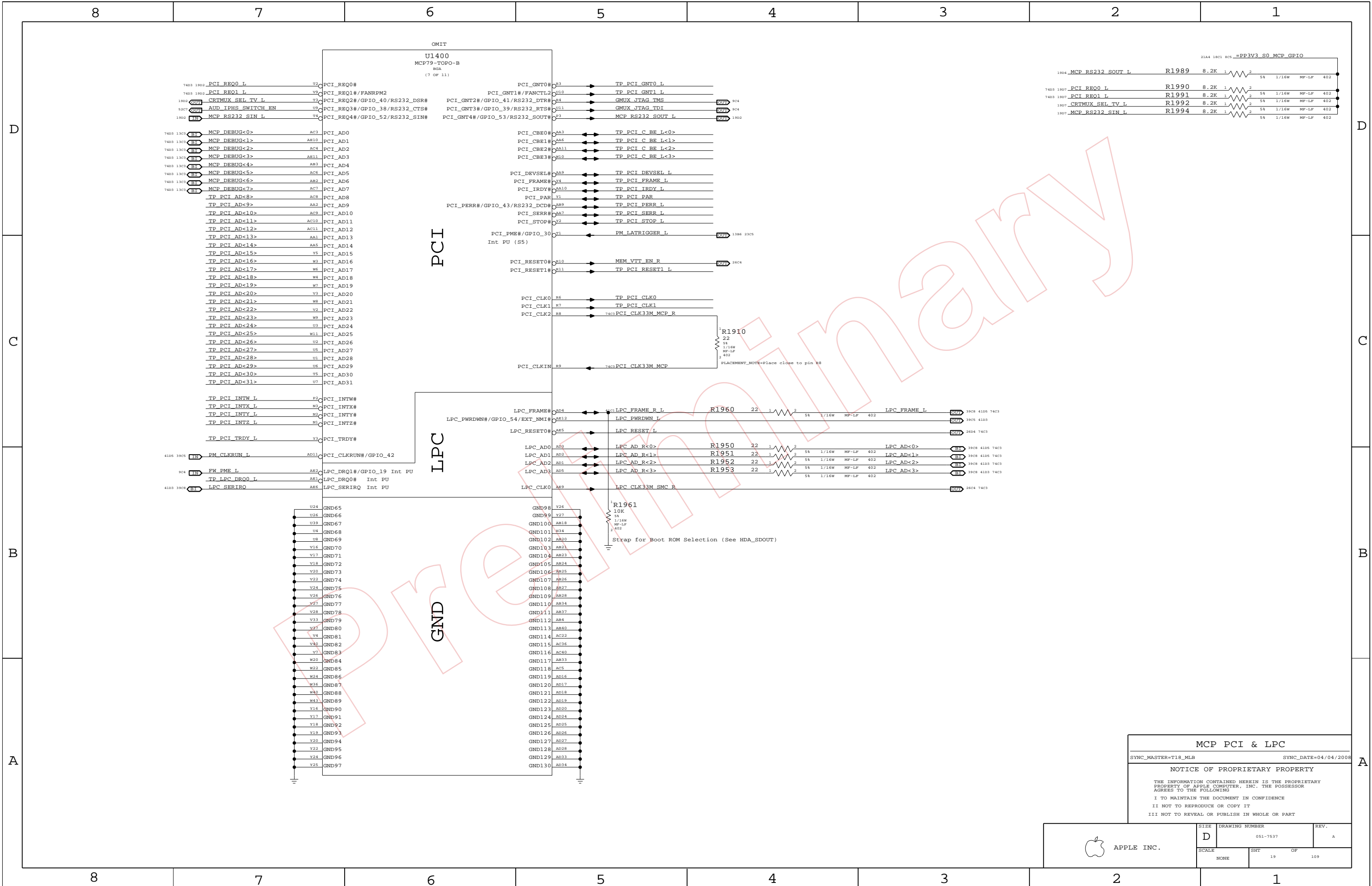
MCP Ethernet & Graphics	
SYNC_MASTER=T18_MLB	SYNC_DATE=04/04/2008
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SCALE	SHT	OF
NONE	18	109





MCP PCI & LPC

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=04/04/2008


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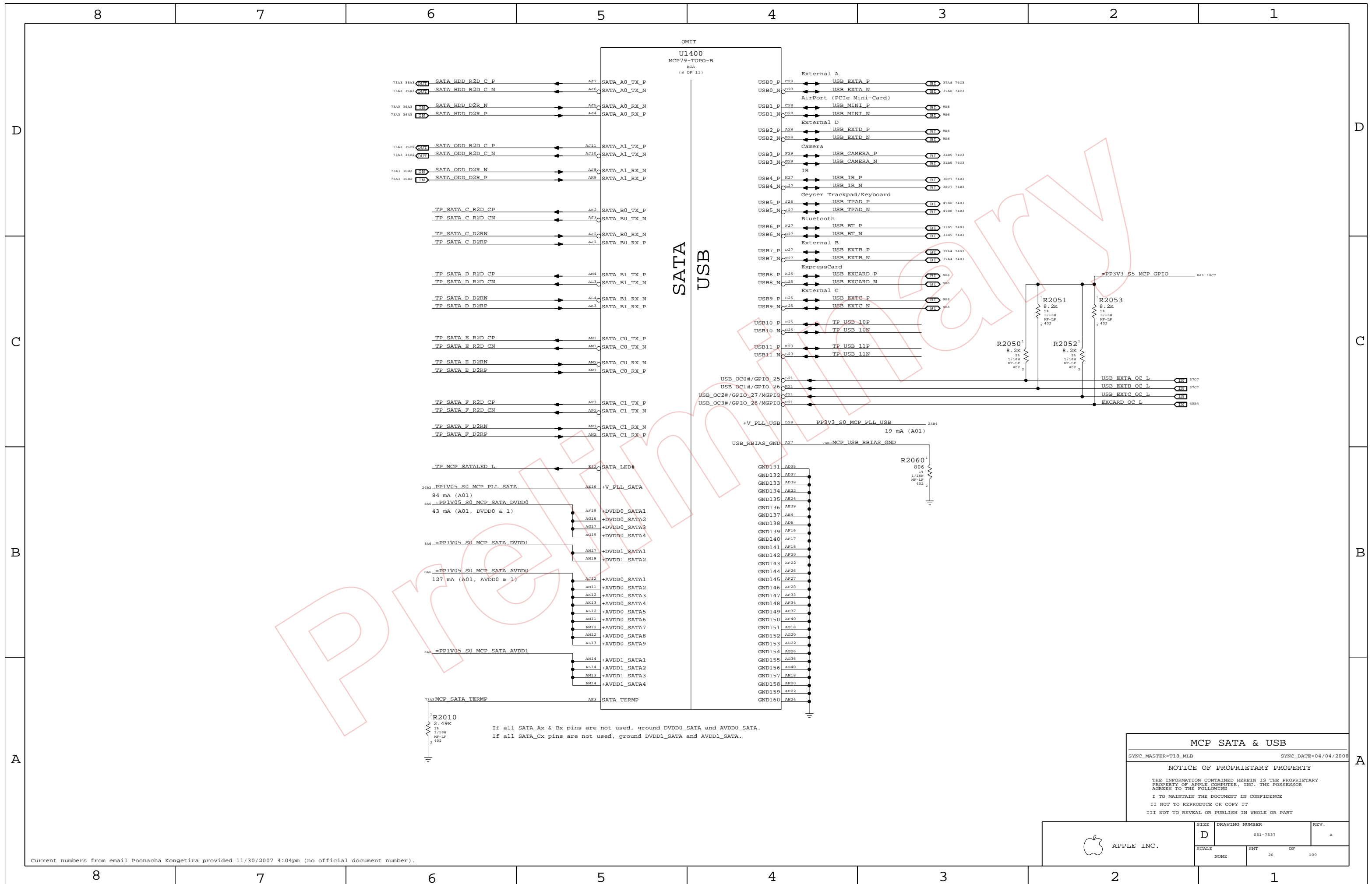
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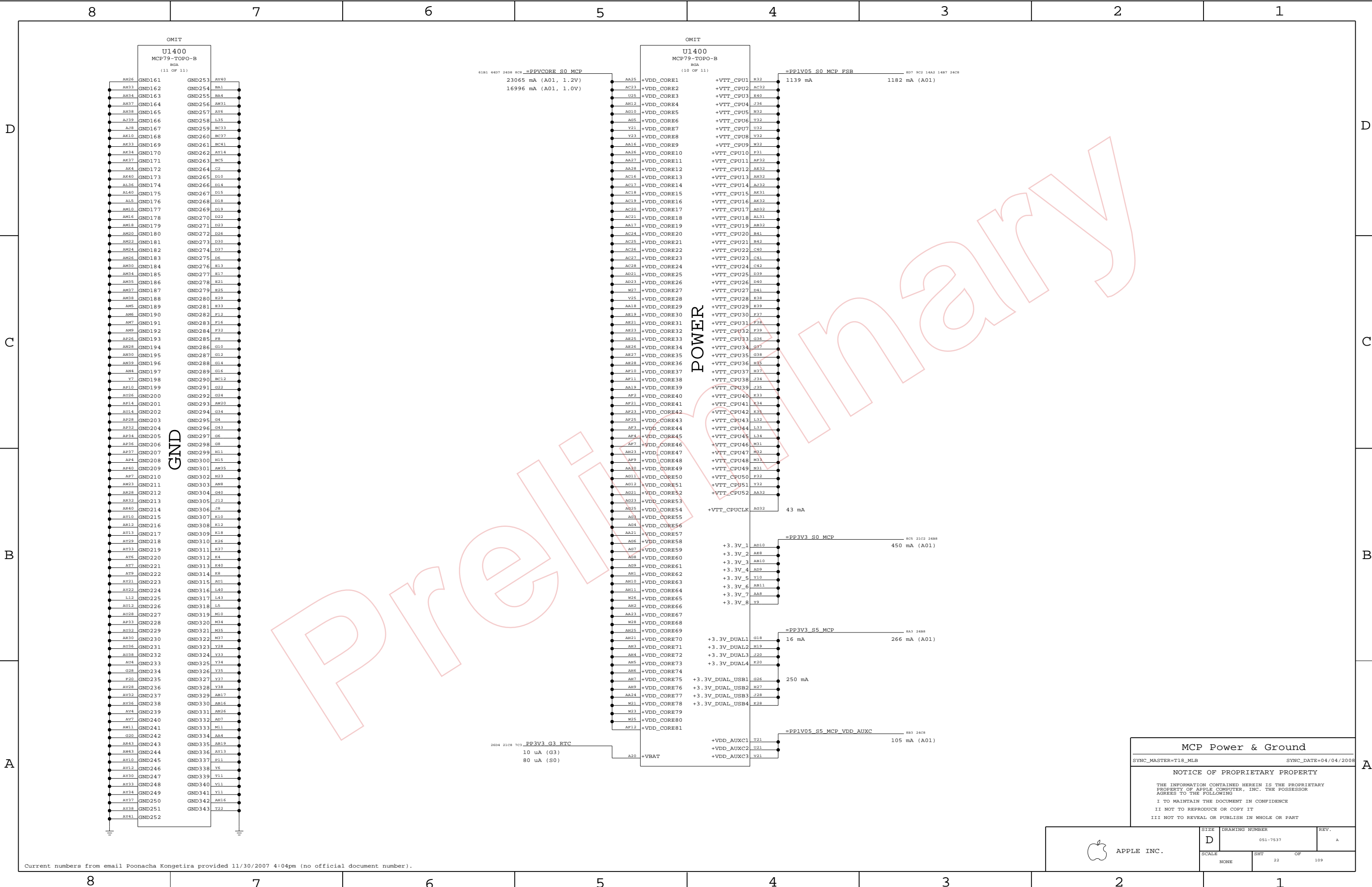
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		19	109







MCP Power & Ground

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=04/04/2008


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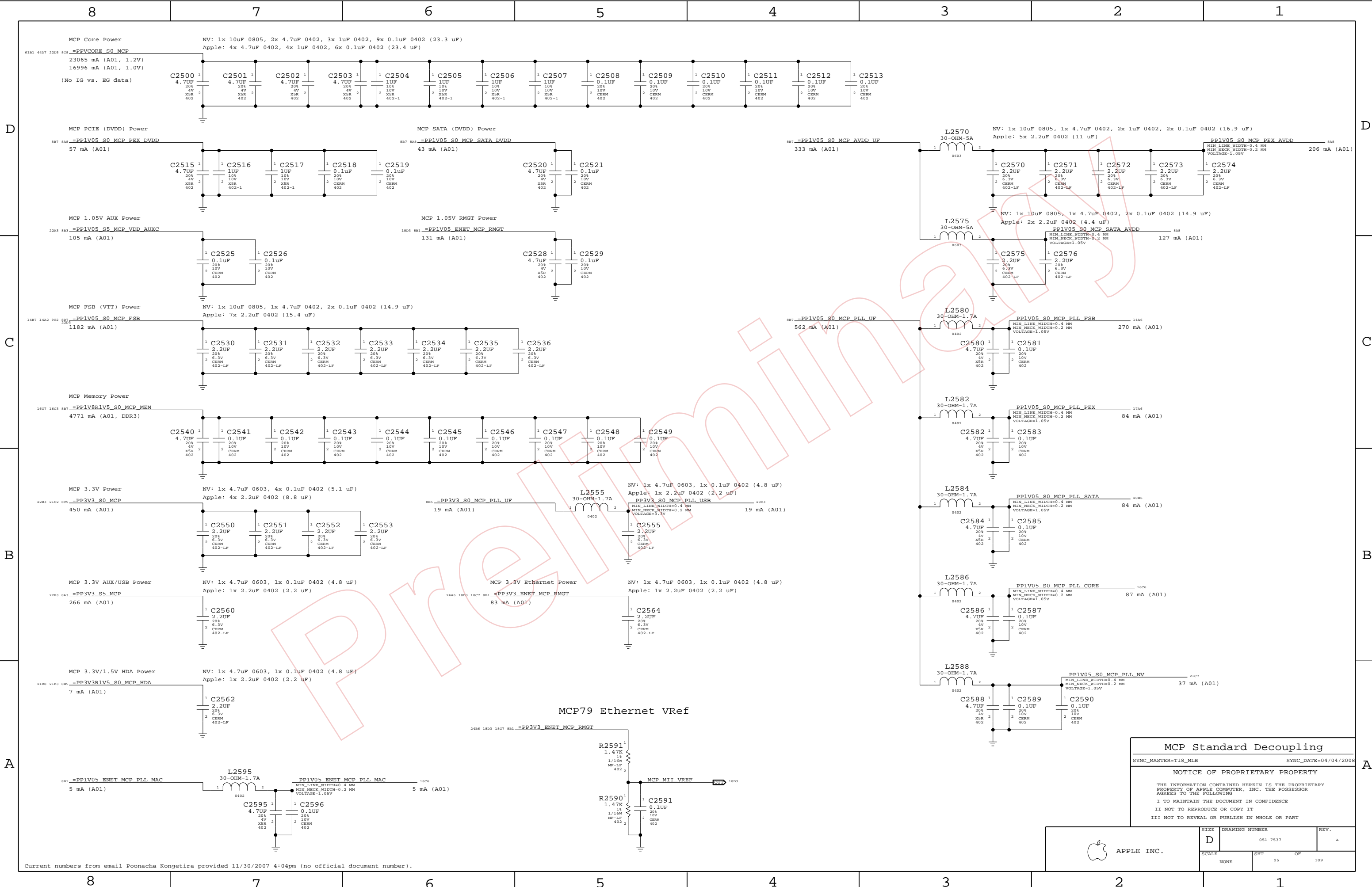
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		22	109



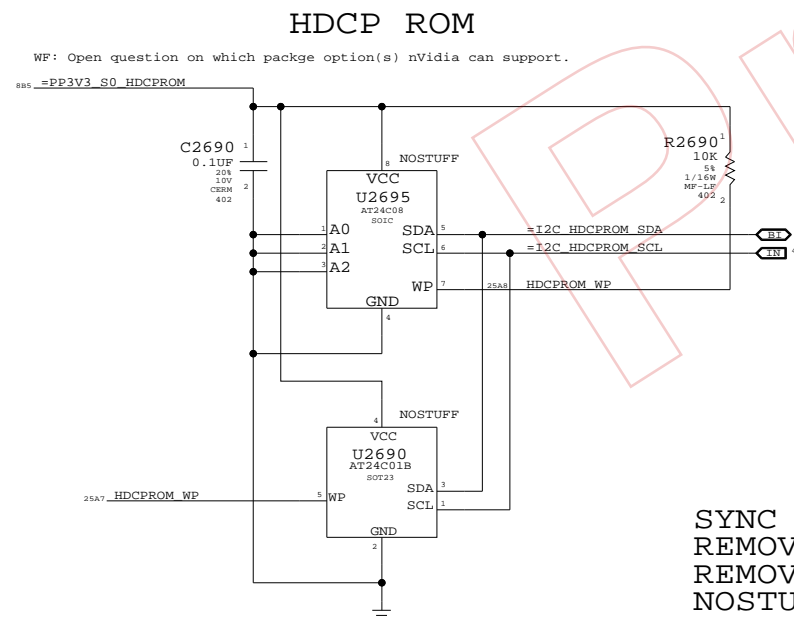
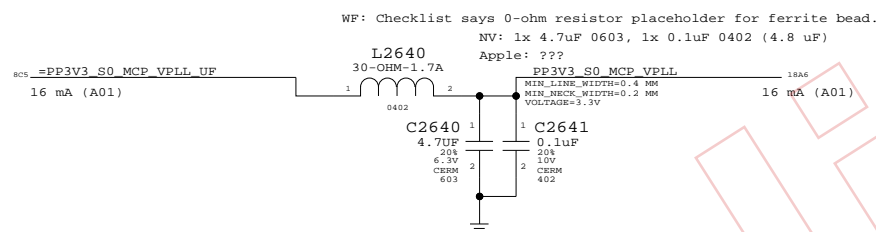
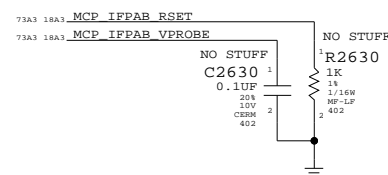
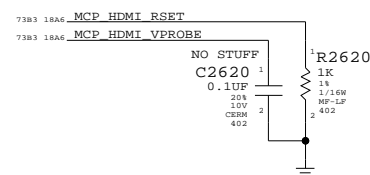
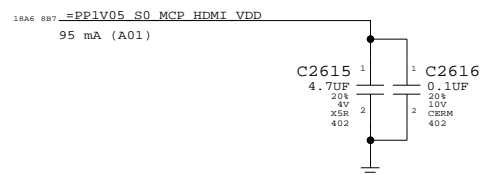
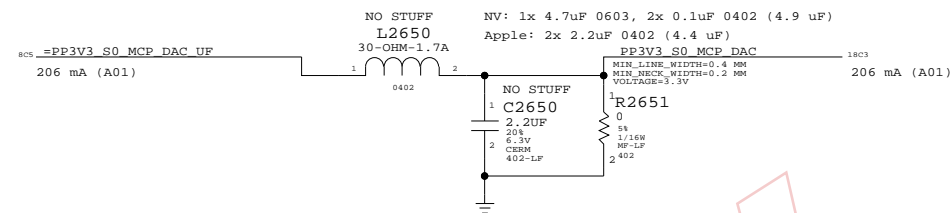
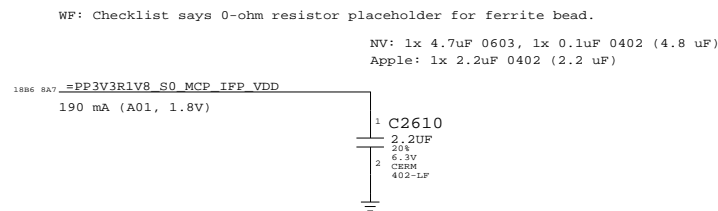




MCP Standard Decoupling		
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	SCALE	SHT	OF
	NONE	25	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).




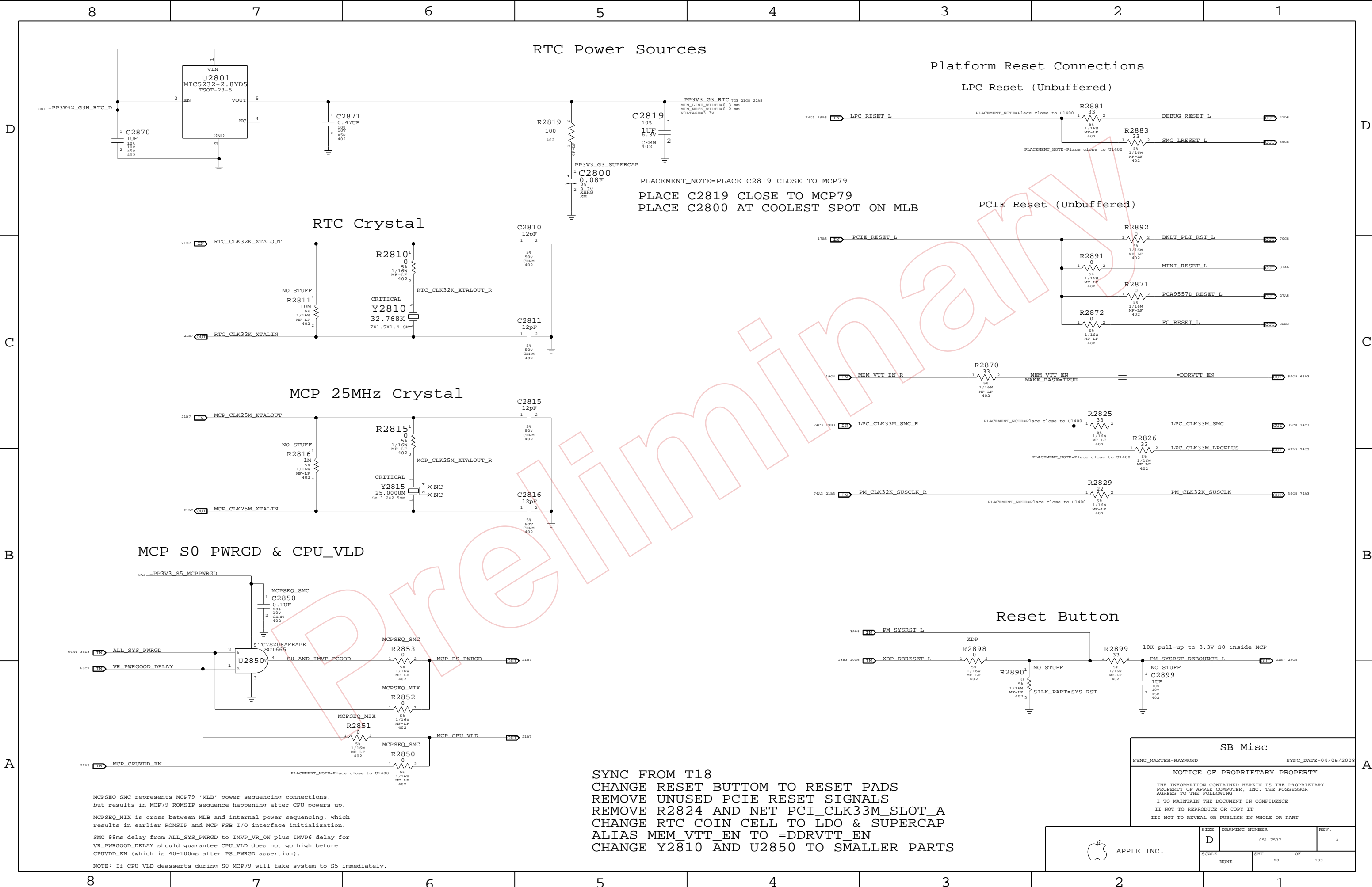
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SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

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MCP Graphics Support	
SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2007
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 APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHT 26 OF 109	



SYNC FROM T18  
CHANGE RESET BUTTON TO RESET PADS  
REMOVE UNUSED PCIE RESET SIGNALS  
REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
CHANGE RTC COIN CELL TO LDO & SUPERCAP  
ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
CHANGE Y2810 AND U2850 TO SMALLER PARTS

Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN
- =PP3V3\_S5\_VREFMRGN
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

- VREFMRGN
- NO\_VREFMRGN

DAC channel  
Min DAC code  
Max DAC code  
Max sink I  
Max source I  
Nominal Vref  
Min Vref  
Max Vref  
Vref Stepping  
(per DAC LSB)

MEM A VREF DQ  
A  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

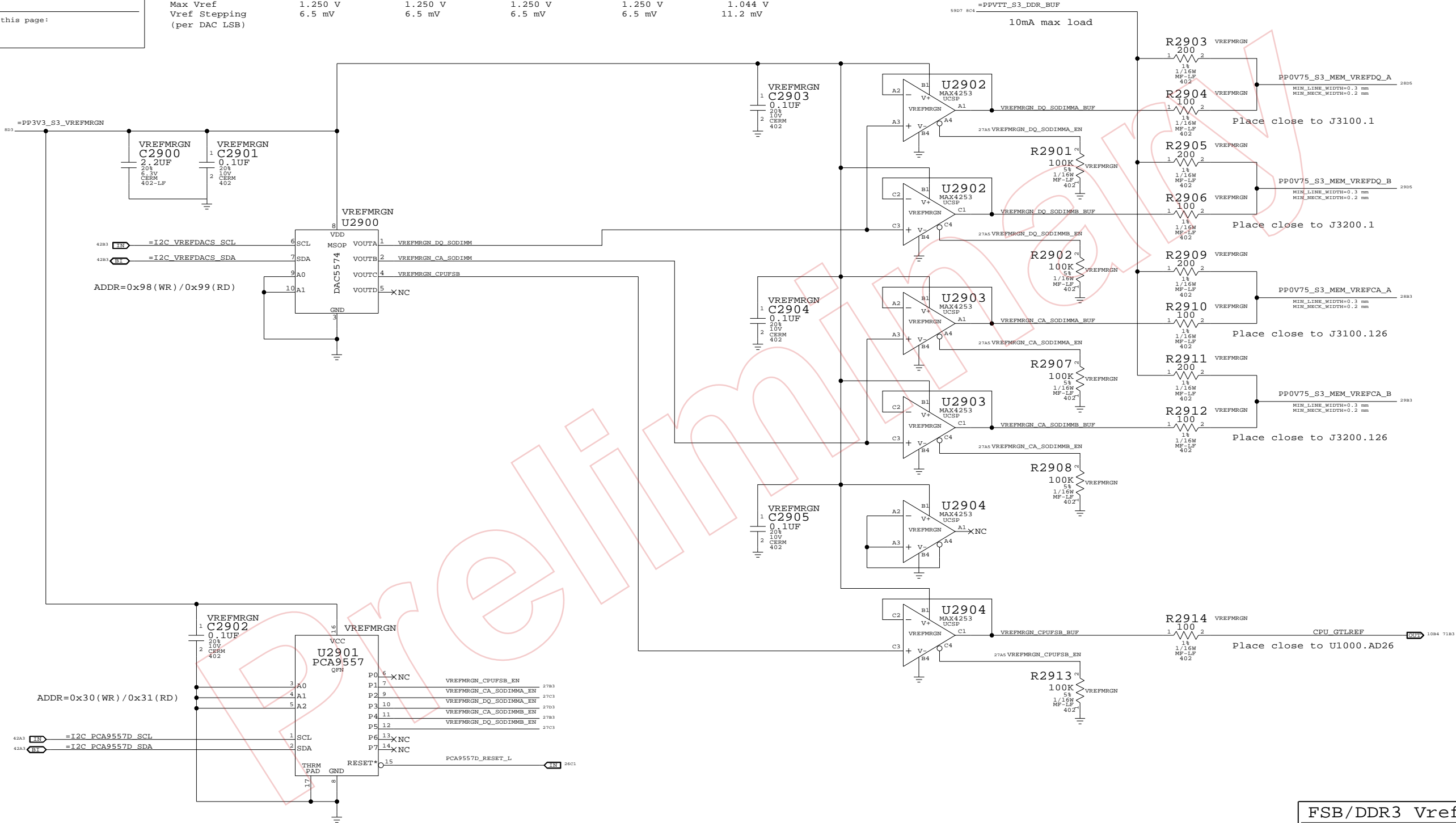
MEM A VREF CA  
B  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

MEM B VREF DQ  
A  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

MEM B VREF CA  
B  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

CPU FSB VREF  
C  
0x00  
0x55  
-0.91 mA  
0.52 mA  
0.70 V  
0.091 V  
1.044 V  
11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately  
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



ADDR=0x30 (WR) / 0x31 (RD)

ADDR=0x98 (WR) / 0x99 (RD)

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC\_MASTER=BEN SYNC\_DATE=03/31/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	29	109

Page Notes

Power aliases required by this page:

- =PP1V5\_S0\_MEM\_A
- =PP1V5\_S3\_MEM\_A
- =PP0V75\_S0\_MEM\_VTT\_A
- =PPSPD\_S0\_MEM\_A (2.5 - 3.3V)

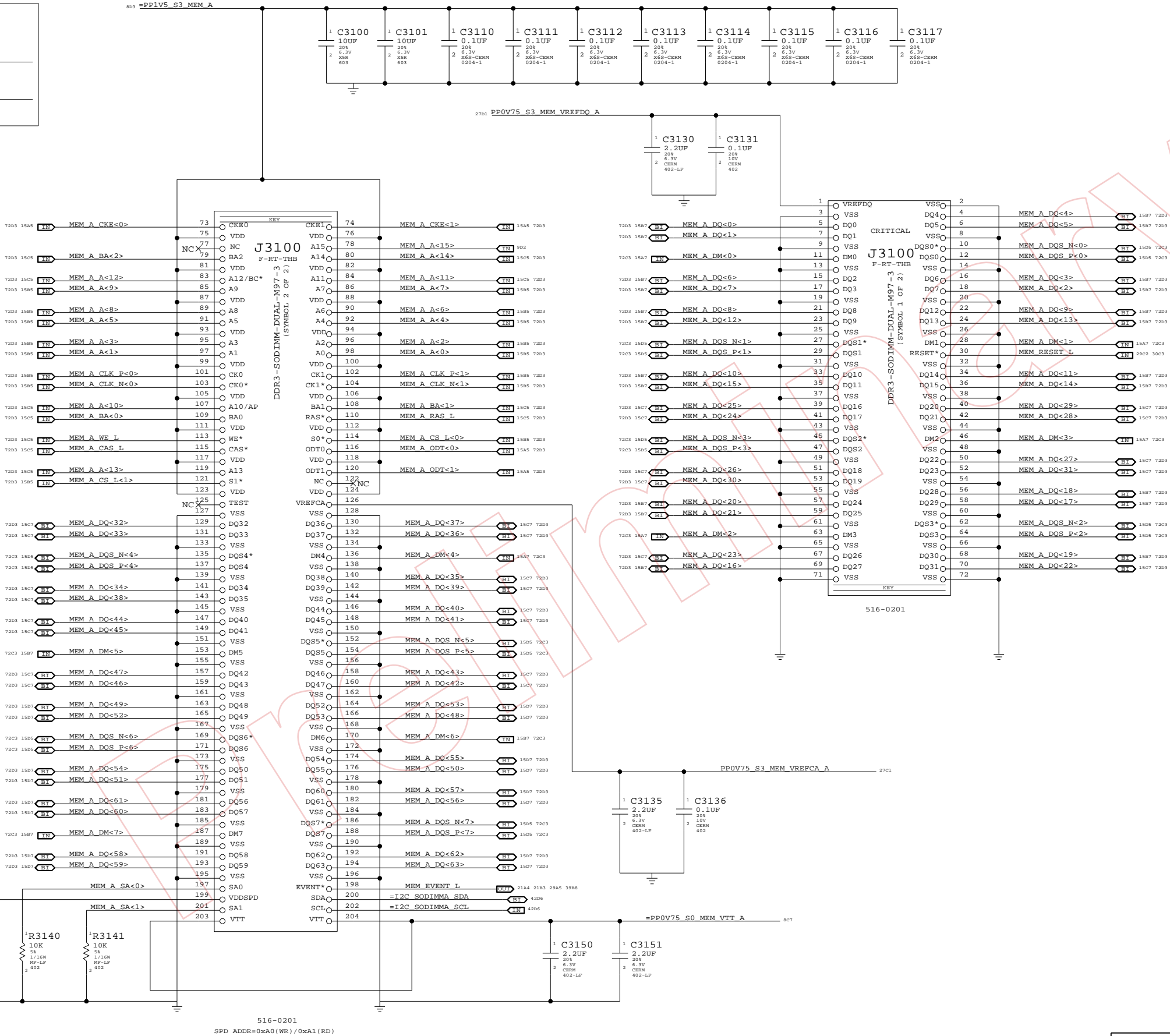
Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC\_MASTER=BIN

SYNC\_DATE=06/30/2008

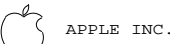
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APPLE INC.

SIZE

DRAWING NUMBER

REV.

D

051-7537

A

SCALE

SHT

OF

109

NONE

31



## Page Notes

Power aliases required by this page:

- =PP1V5\_S0\_MEM\_B  
- =PP1V5\_S3\_MEM\_B  
- =PP0V75\_S0\_MEM\_VTT\_B  
- =PPSPD\_S0\_MEM\_B (2.5 - 3.3V)

Signal aliases required by this page:

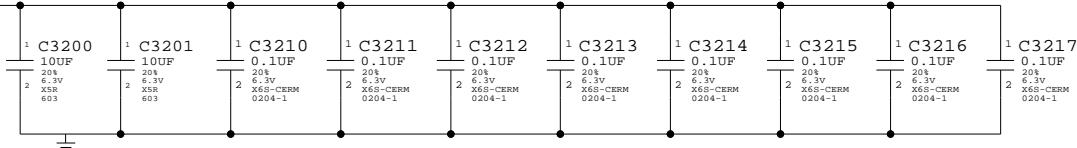
- =I2C\_SODIMMB\_SCL  
- =I2C\_SODIMMB\_SDA

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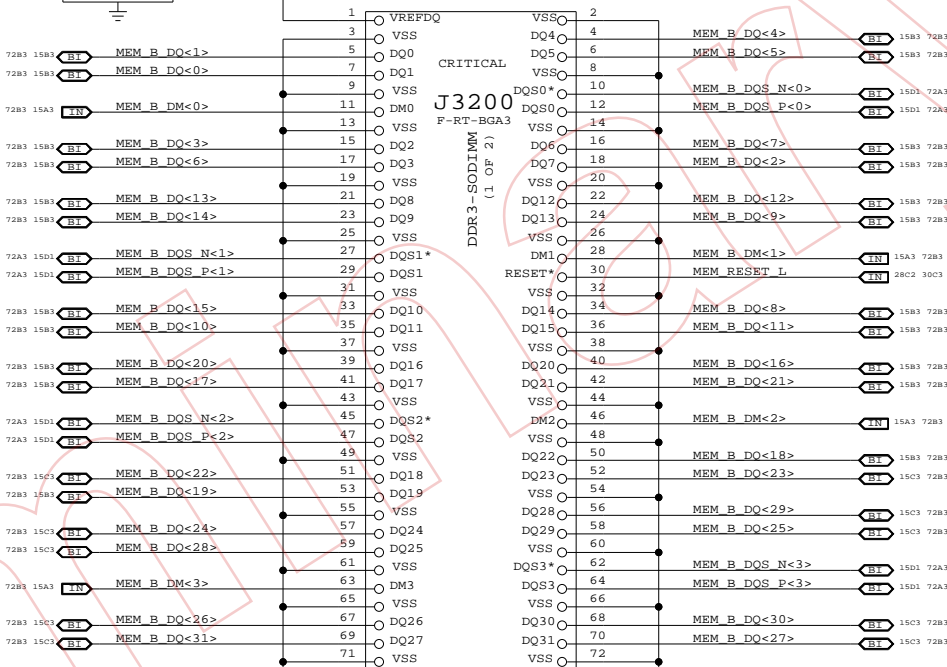
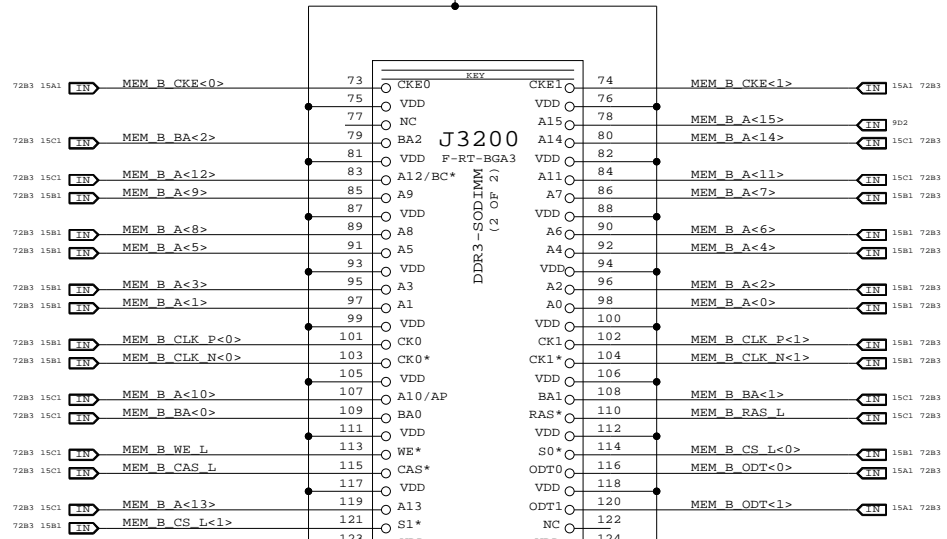
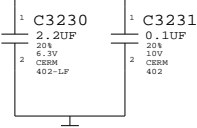
(NONE)

## DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

803 =PP1V5\_S3\_MEM\_B



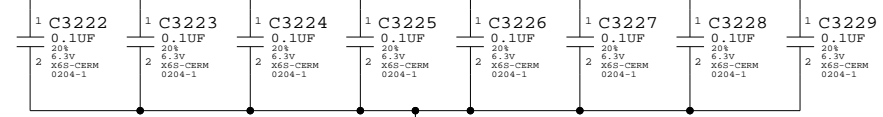
2701 PP0V75\_S3\_MEM\_VREFDQ\_B



516S0706

## DDR3 GROUND RETURN CAPS (MCP SIDE)

887 =PP1V5\_S0\_MEM\_MCP



807 =PP0V75\_S0\_MEM\_VTT\_B



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

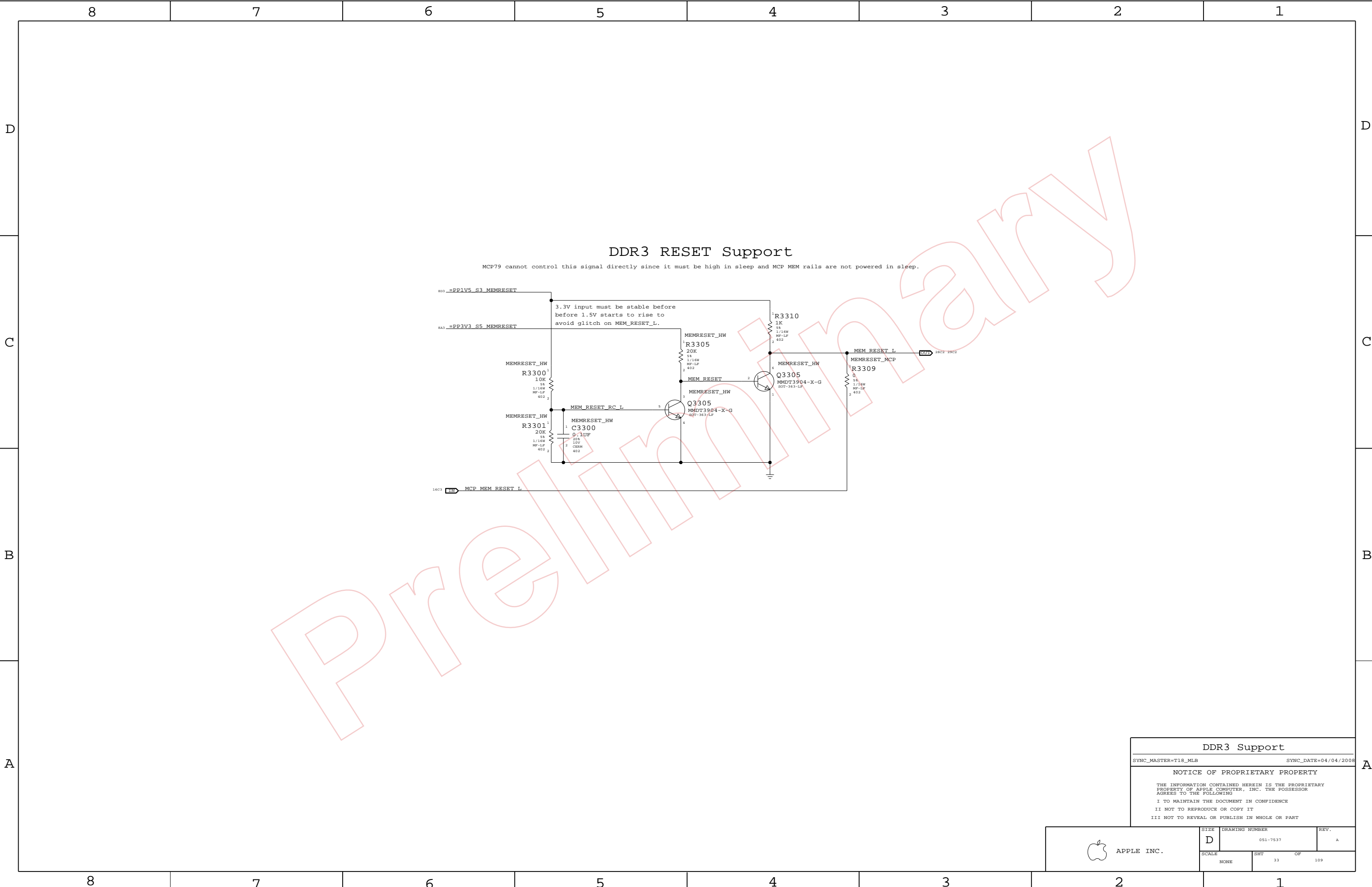
SYNC\_MASTER=BBN SYNC\_DATE=05/09/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	32	109



DDR3 Support

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=04/04/2008

NOTICE OF PROPRIETARY PROPERTY

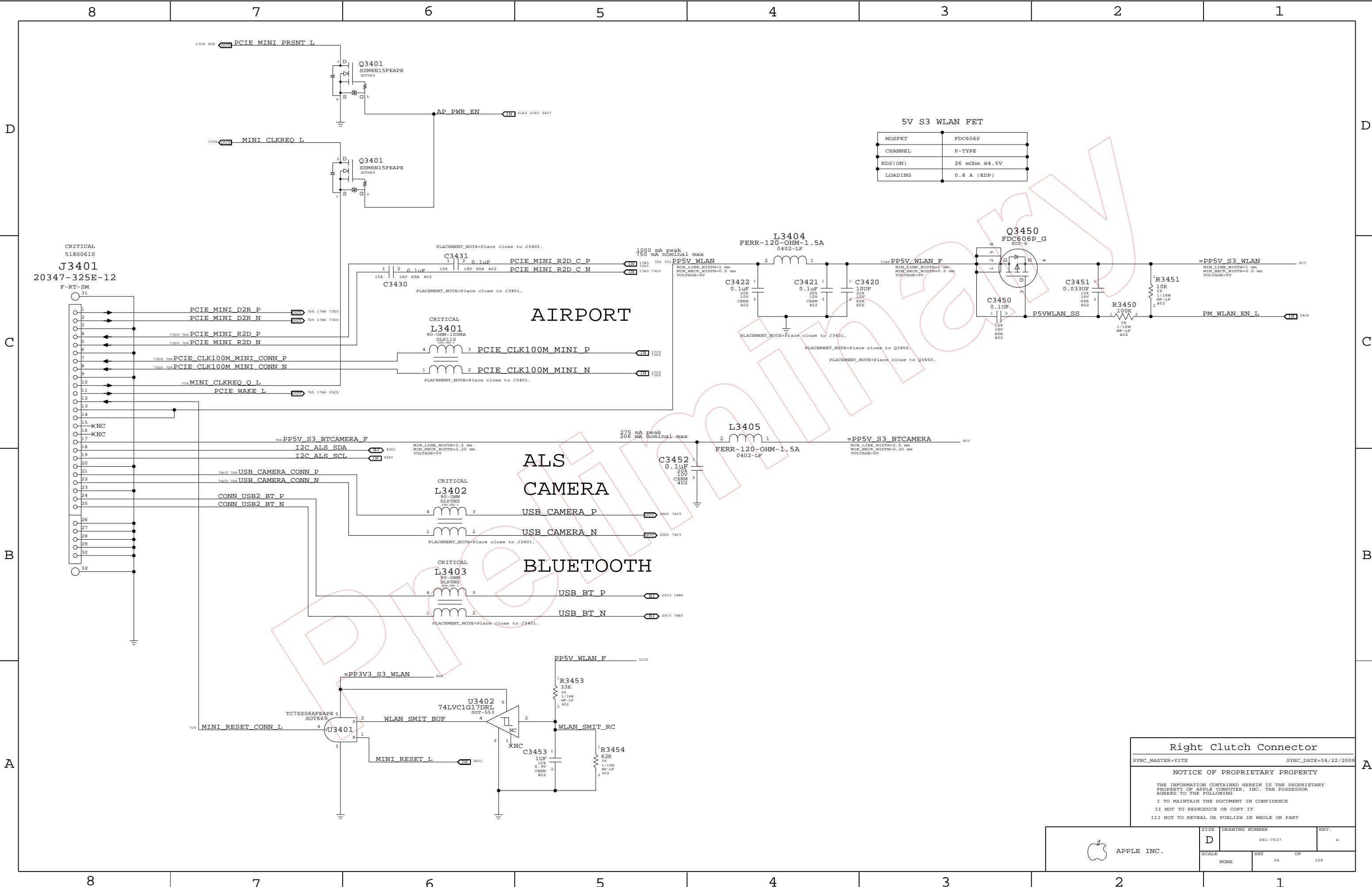
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	NONE	SHT	OF
		33	109



5V S3 WLAN FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Right Clutch Connector

SYNC\_MASTER=YITE

SYNC\_DATE=04/22/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	NONE	SHT	OF
		34	109



D

C

B

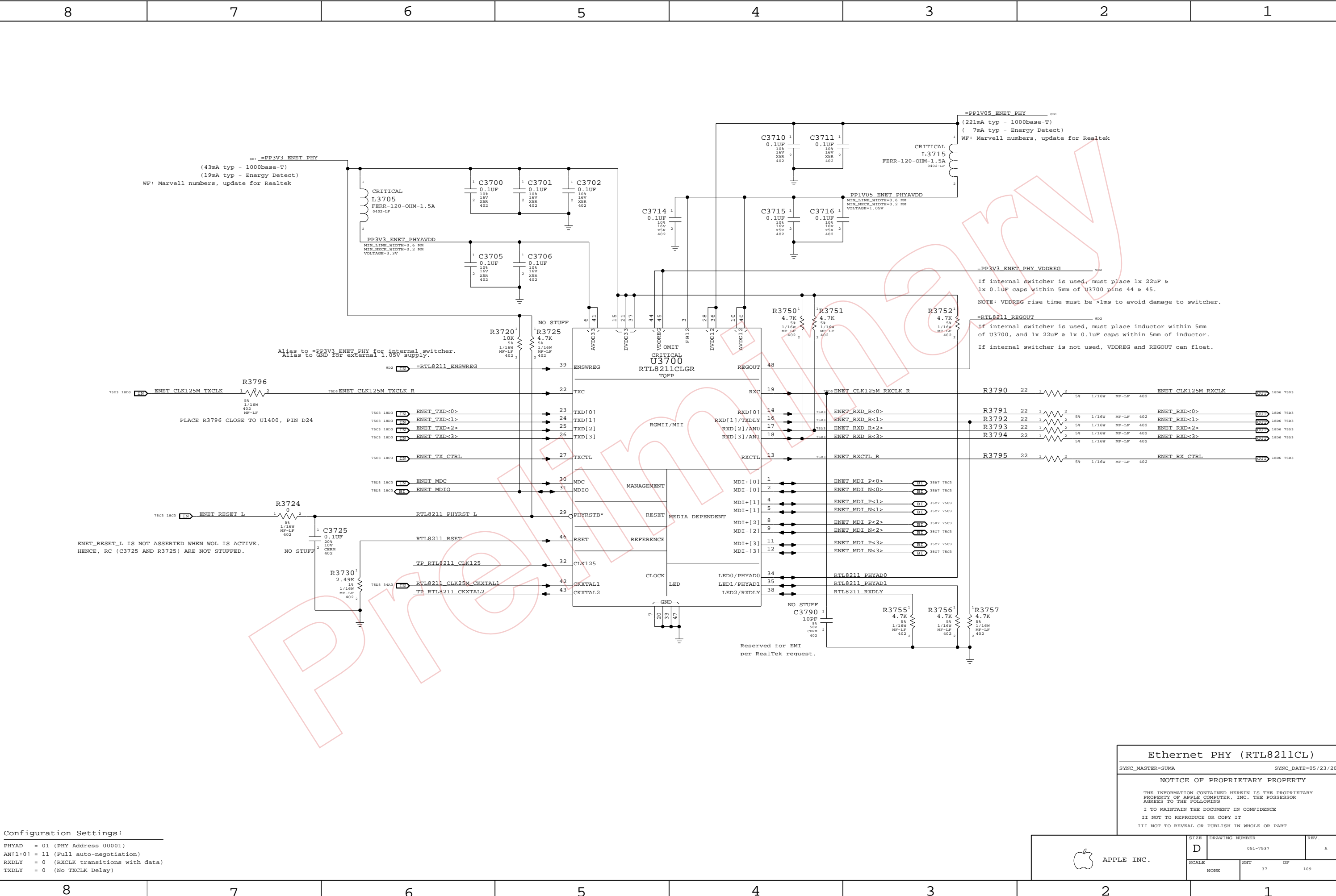
A

D

C

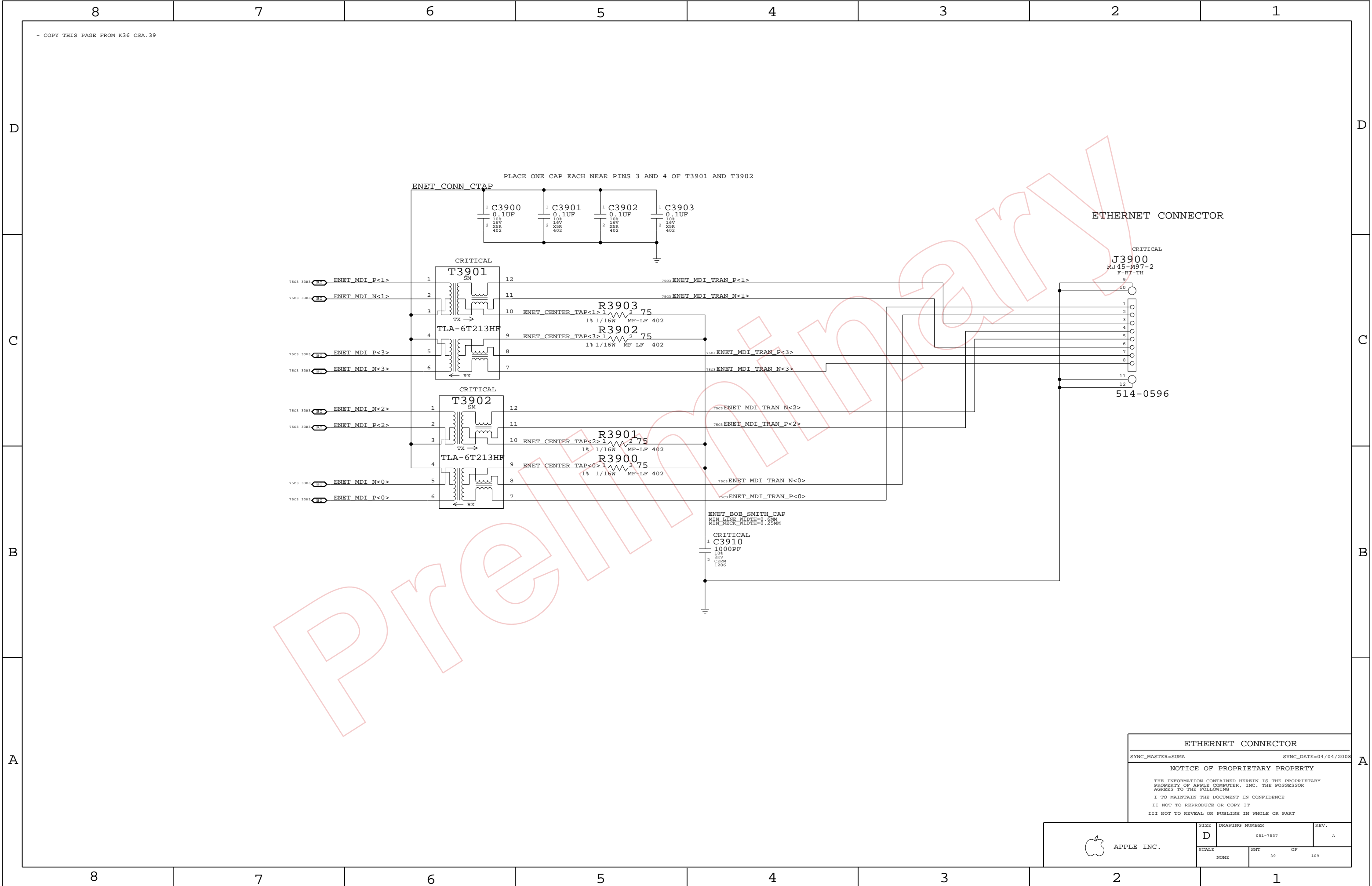
B

A



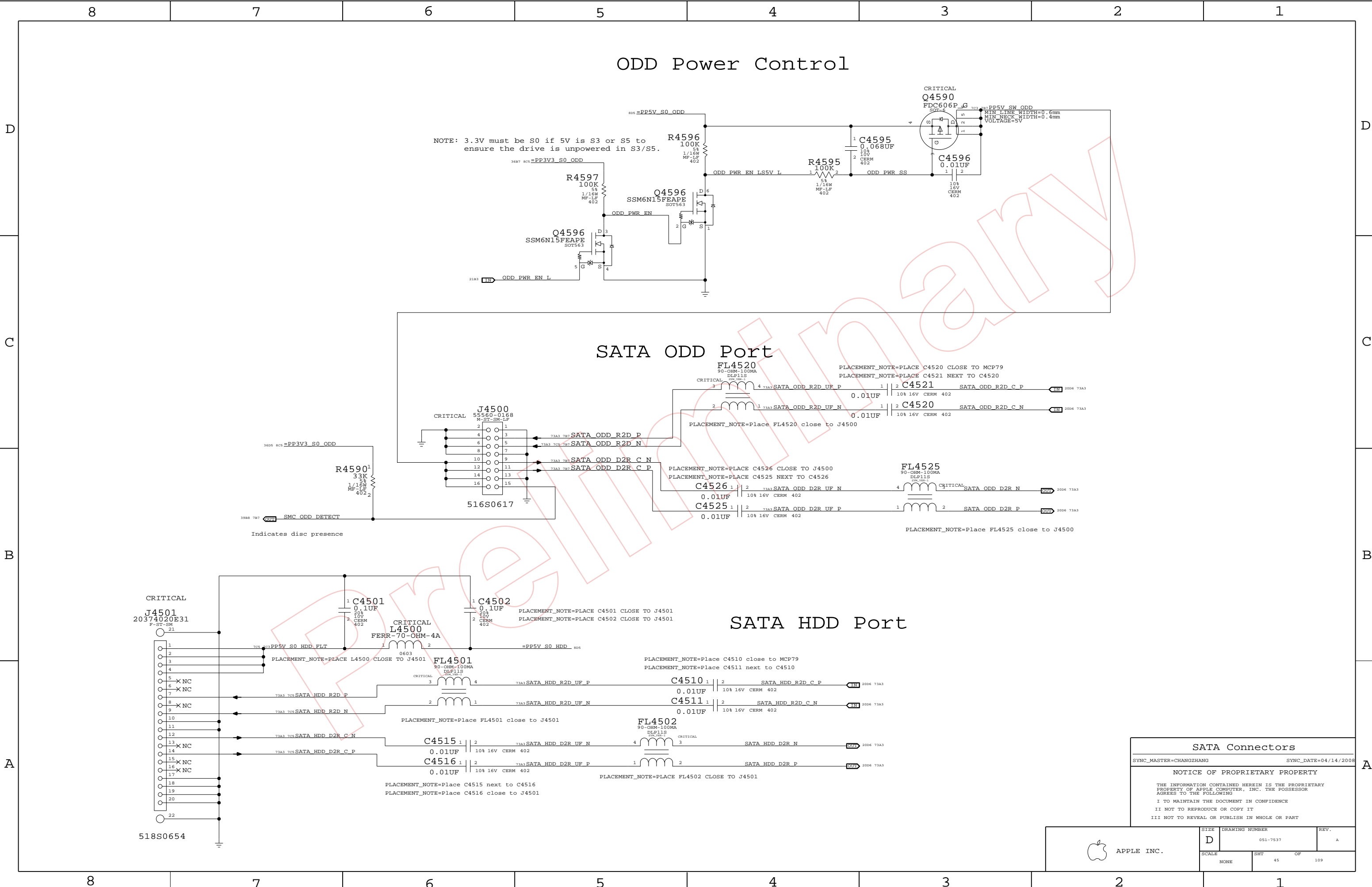







ETHERNET CONNECTOR		
SYNC_MASTER=SUMA		SYNC_DATE=04/04/2008
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHT 39	OF 109



SATA Connectors		
SYNC_MASTER=CHANGZHANG		SYNC_DATE=04/14/2008
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		45	109

Port Power Switch

USB PORT A (FRONT PORT)

USB/SMC Debug Mux

USB PORT B (BACK PORT)

External USB Connectors

SYNC\_MASTER=YUAN.MA

SYNC\_DATE=01/18/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7537

REV.

A

SCALE

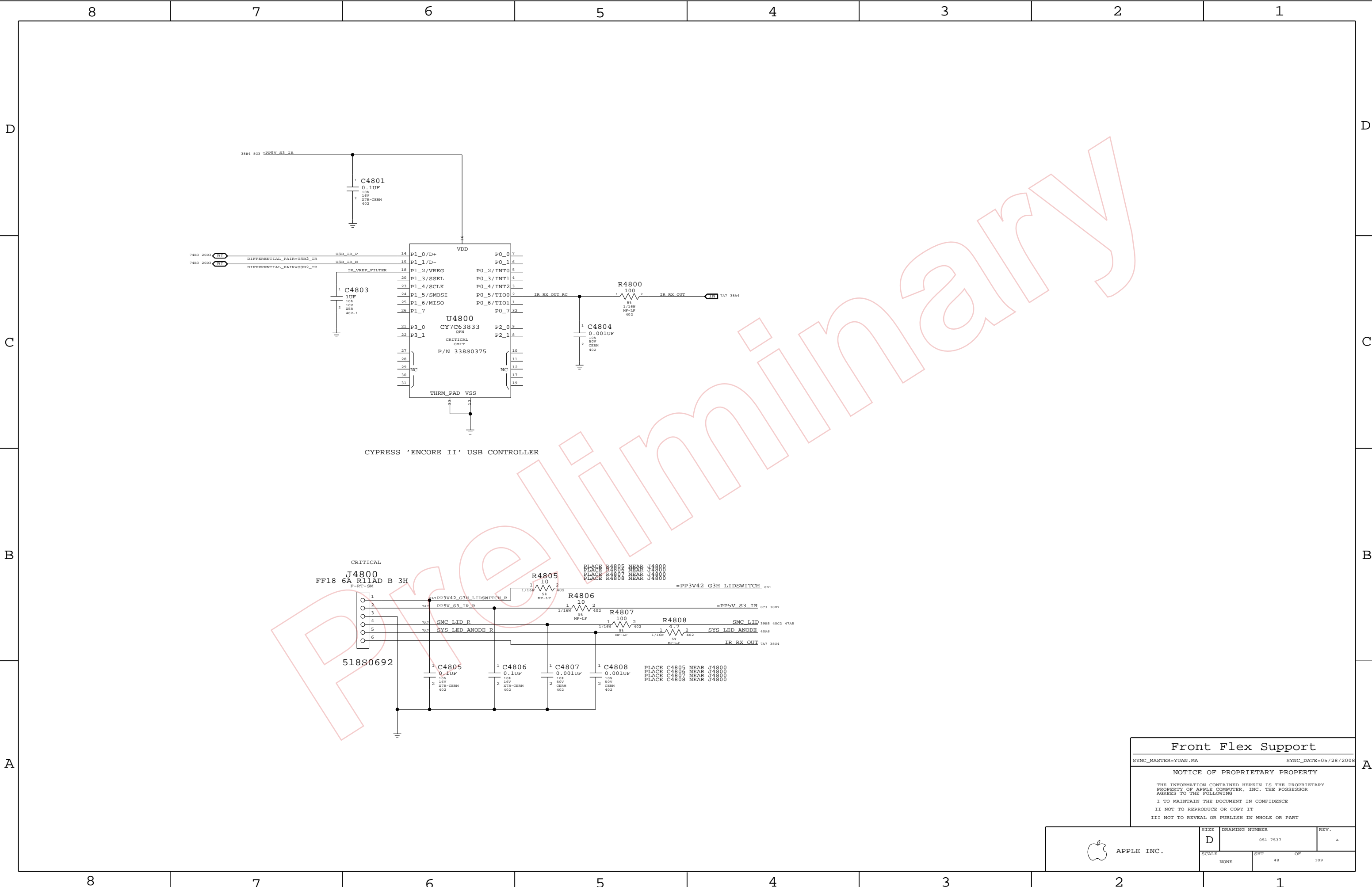
NONE

SHT

46

OF

109



Front Flex Support

SYNC\_MASTER=YUAN.MA SYNC\_DATE=05/28/2008

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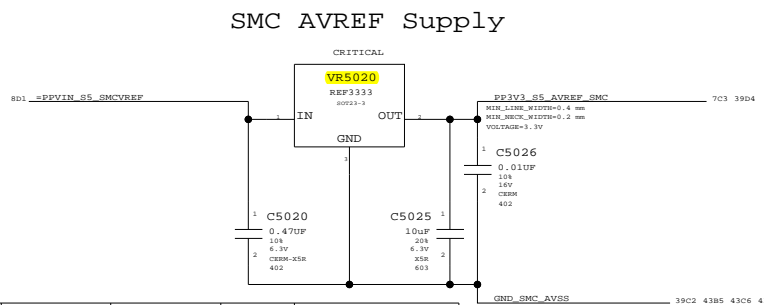
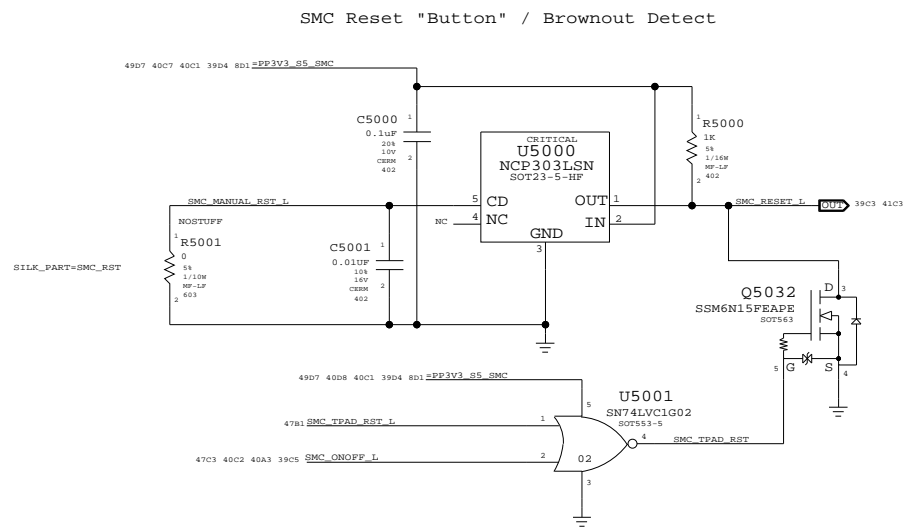
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

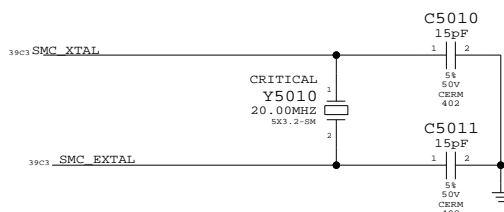
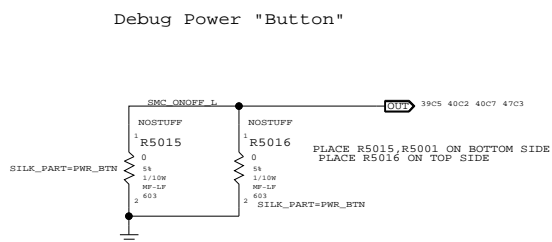
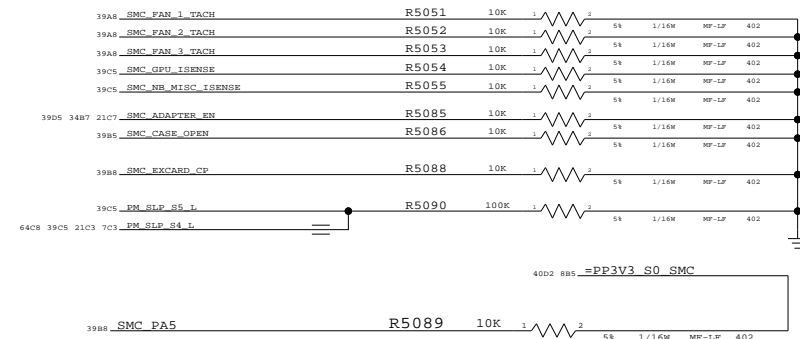
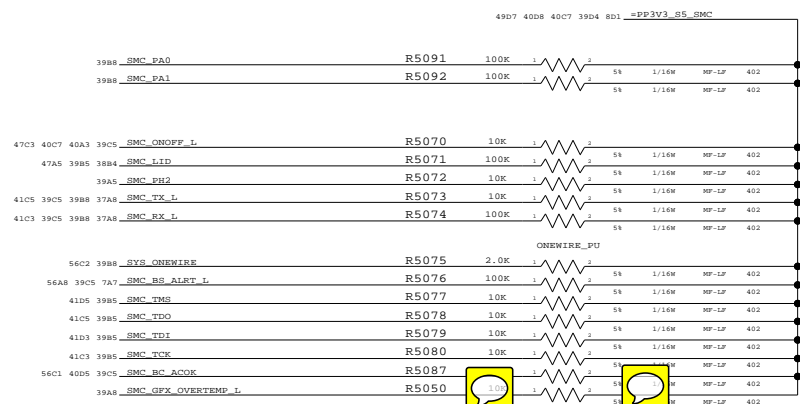
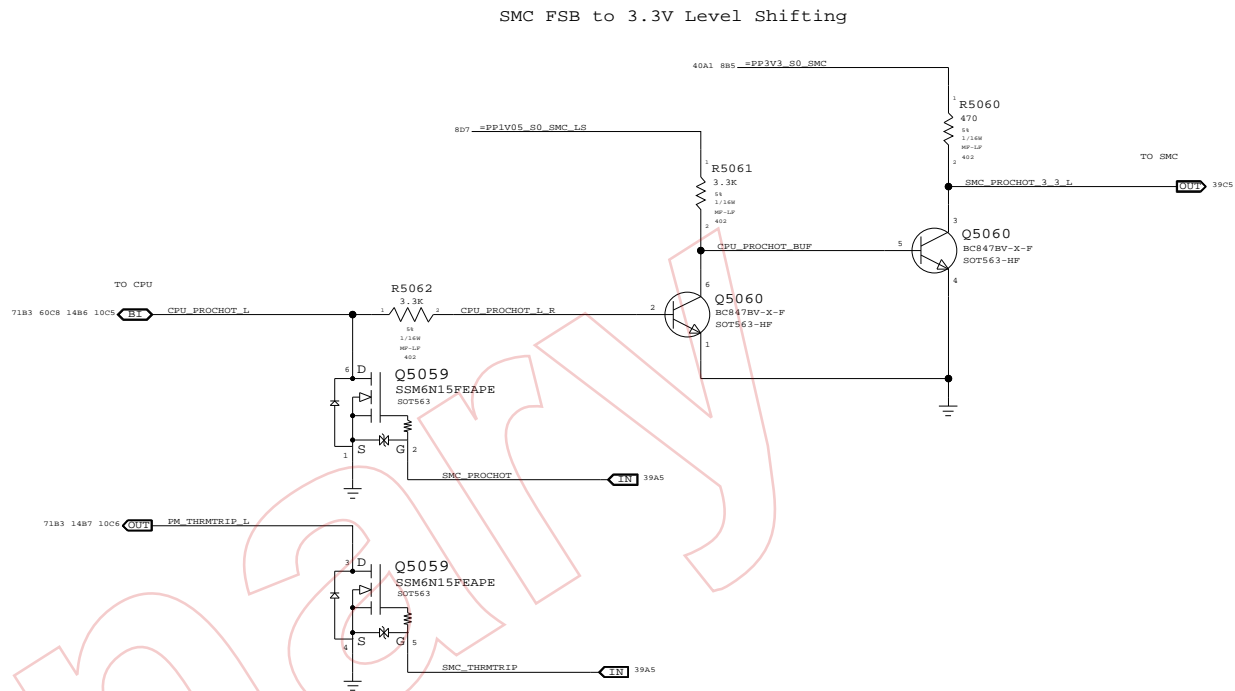
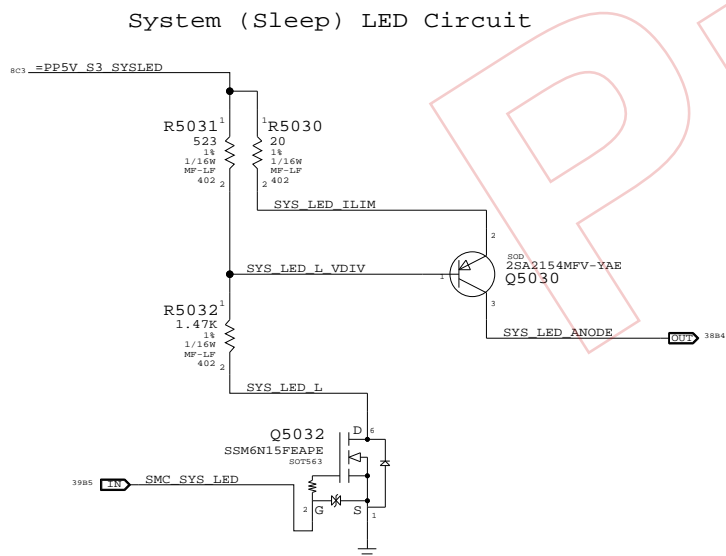
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		48	109







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Internsl ISL60002-33



SMC Support	
SYNC_MASTER=YUAN.MA	SYNC_DATE=05/28/2008
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8	7	6	5	4	3	2	1
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## C

B




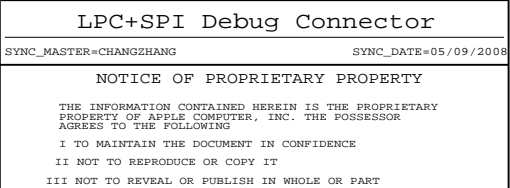
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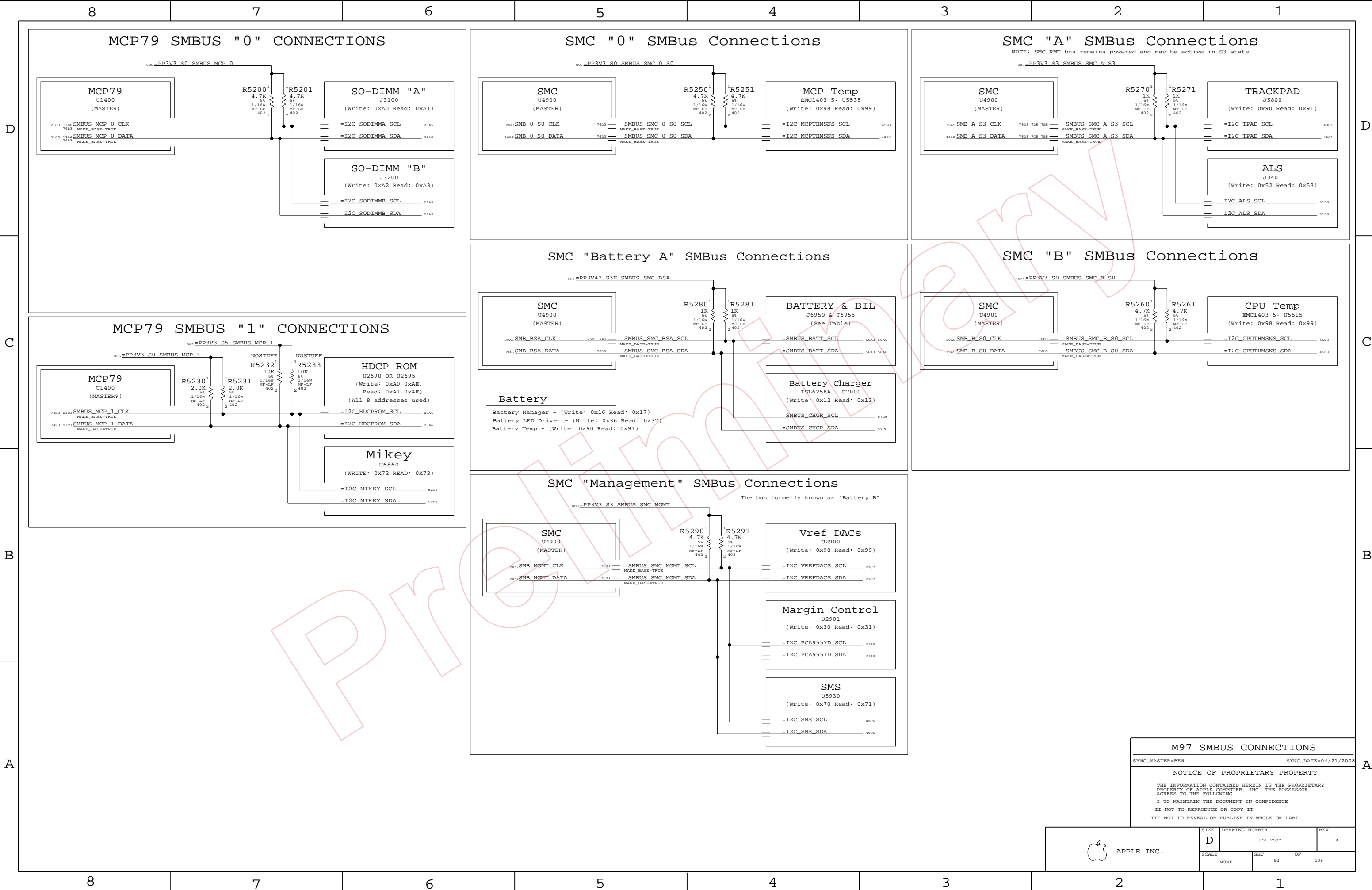
C



## A

68D8 64D5 39C5 34B7 21C3 7C3  PM SLP S3 L 1 0 2 MCP SPI FORCE L  
5%  
1/16W  
MF-LF  
402





M97 SMBUS CONNECTIONS

SYNC\_MASTER=BEN SYNC\_DATE=04/21/2008

NOTICE OF PROPRIETARY PROPERTY

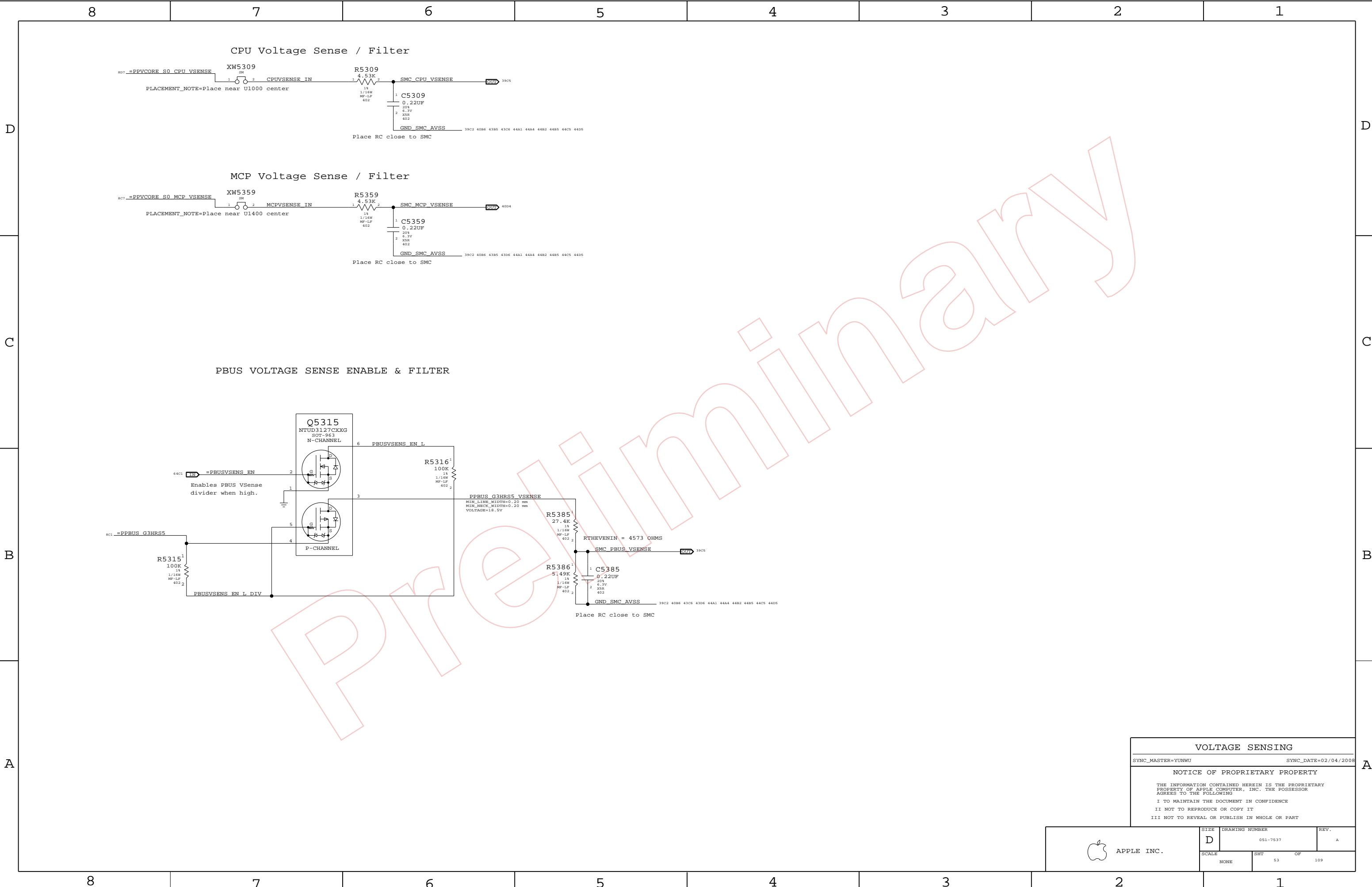
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		52	109



VOLTAGE SENSING

SYNC\_MASTER=YUNWU

SYNC\_DATE=02/04/2008


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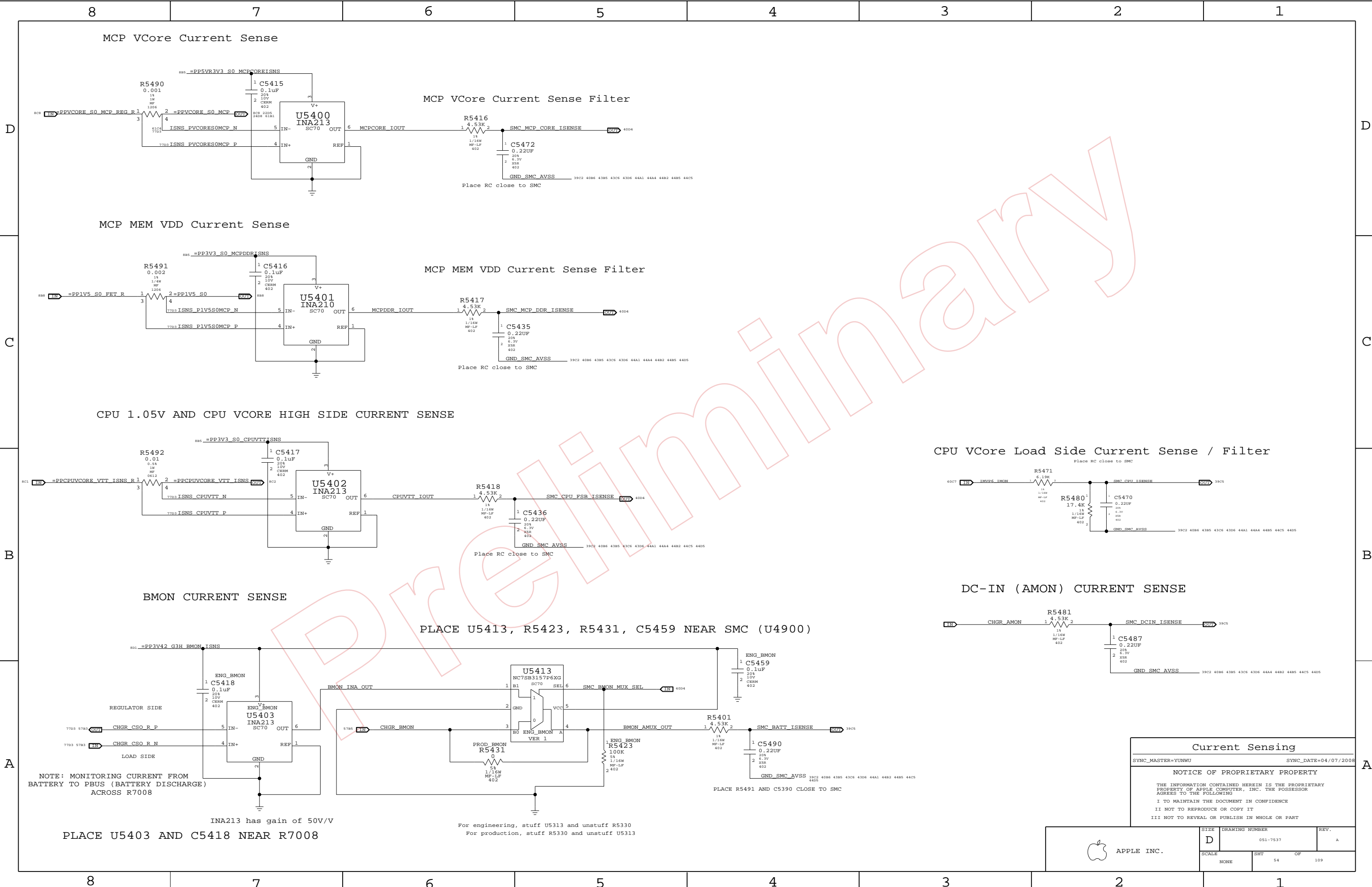
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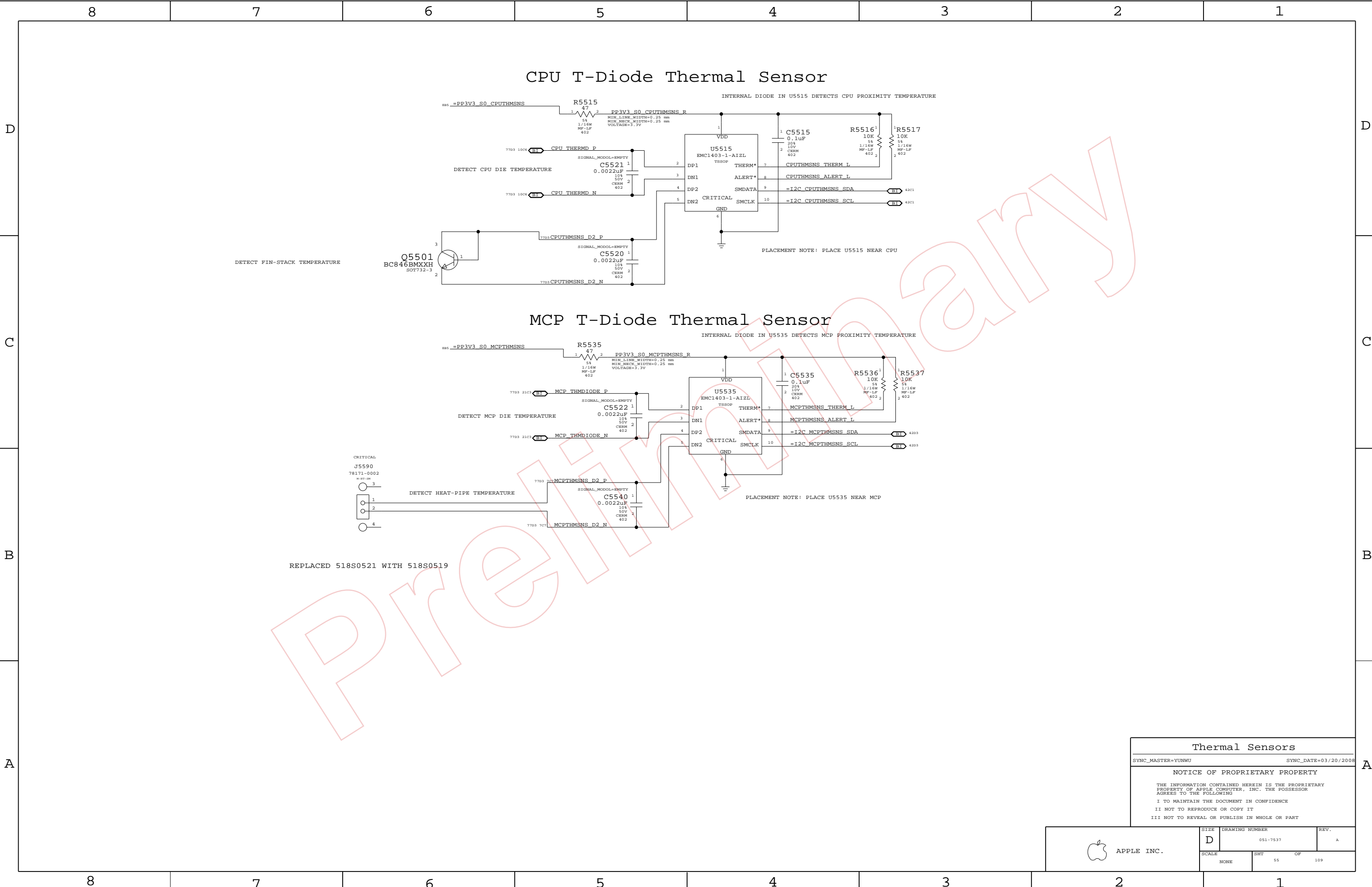
II NOT TO REPRODUCE OR COPY IT

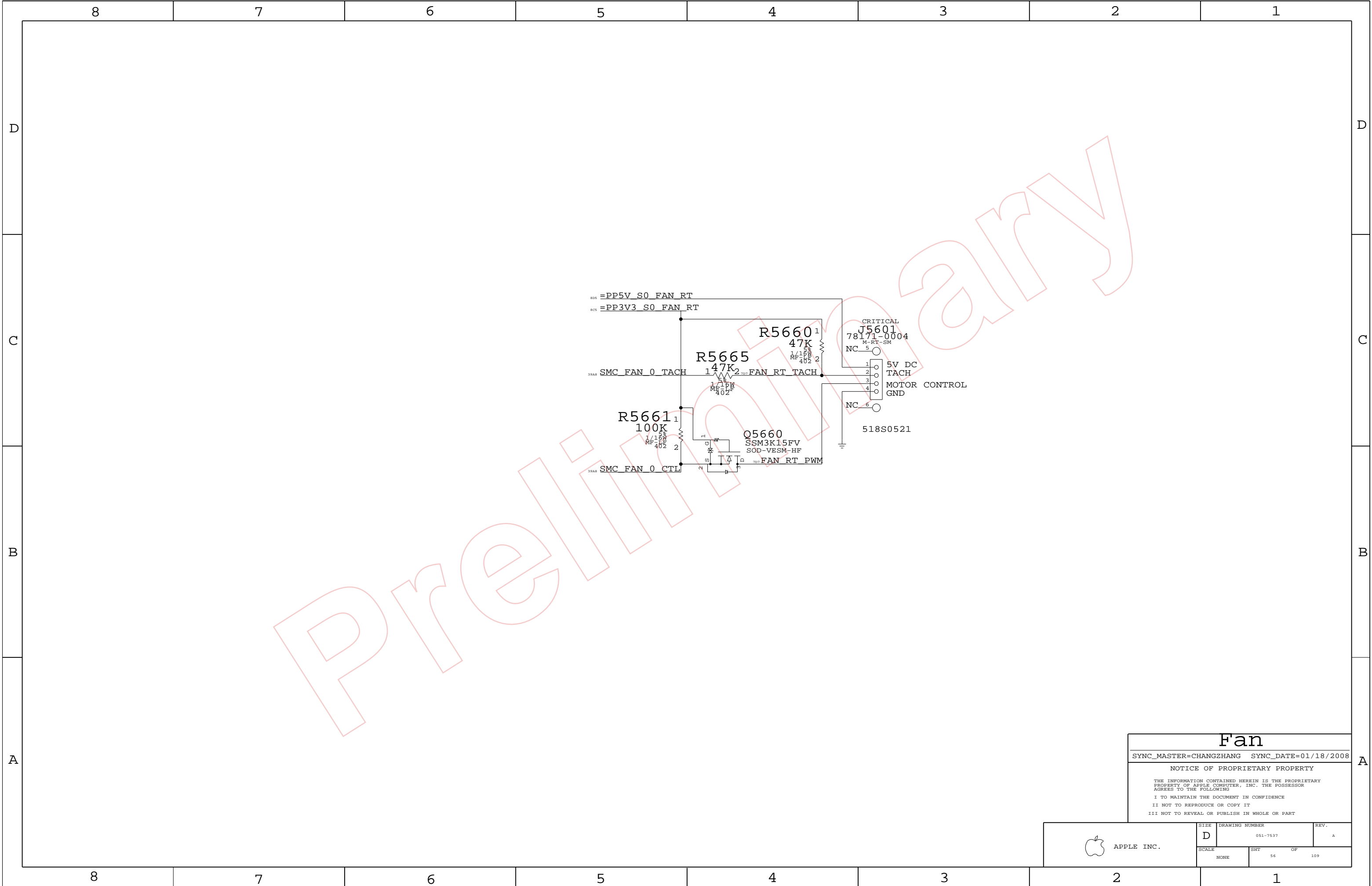
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		53	109









Fan

SYNC\_MASTER=CHANGZHANG SYNC\_DATE=01/18/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7537

REV.

A

SCALE

NONE

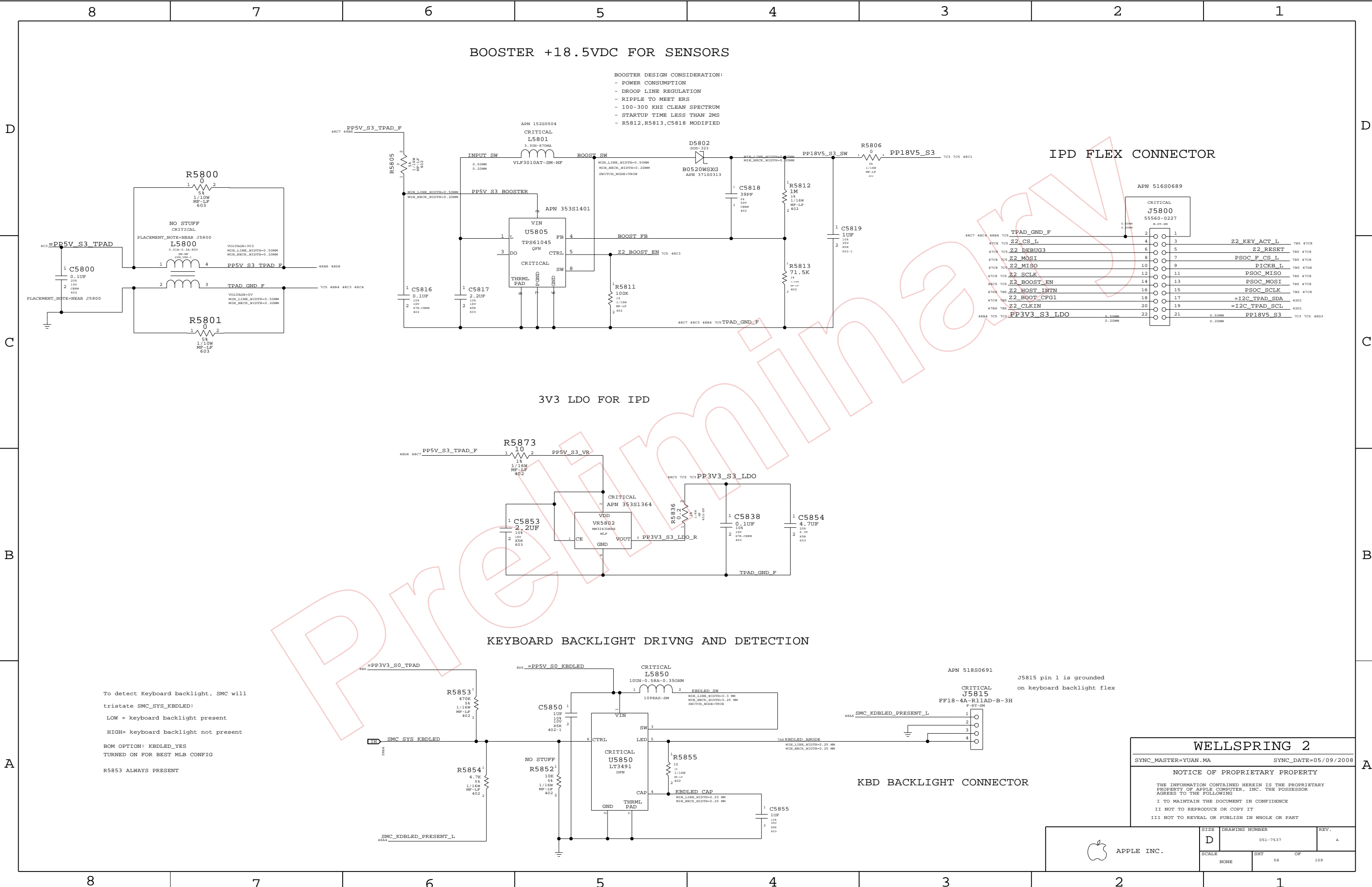
SHT

56

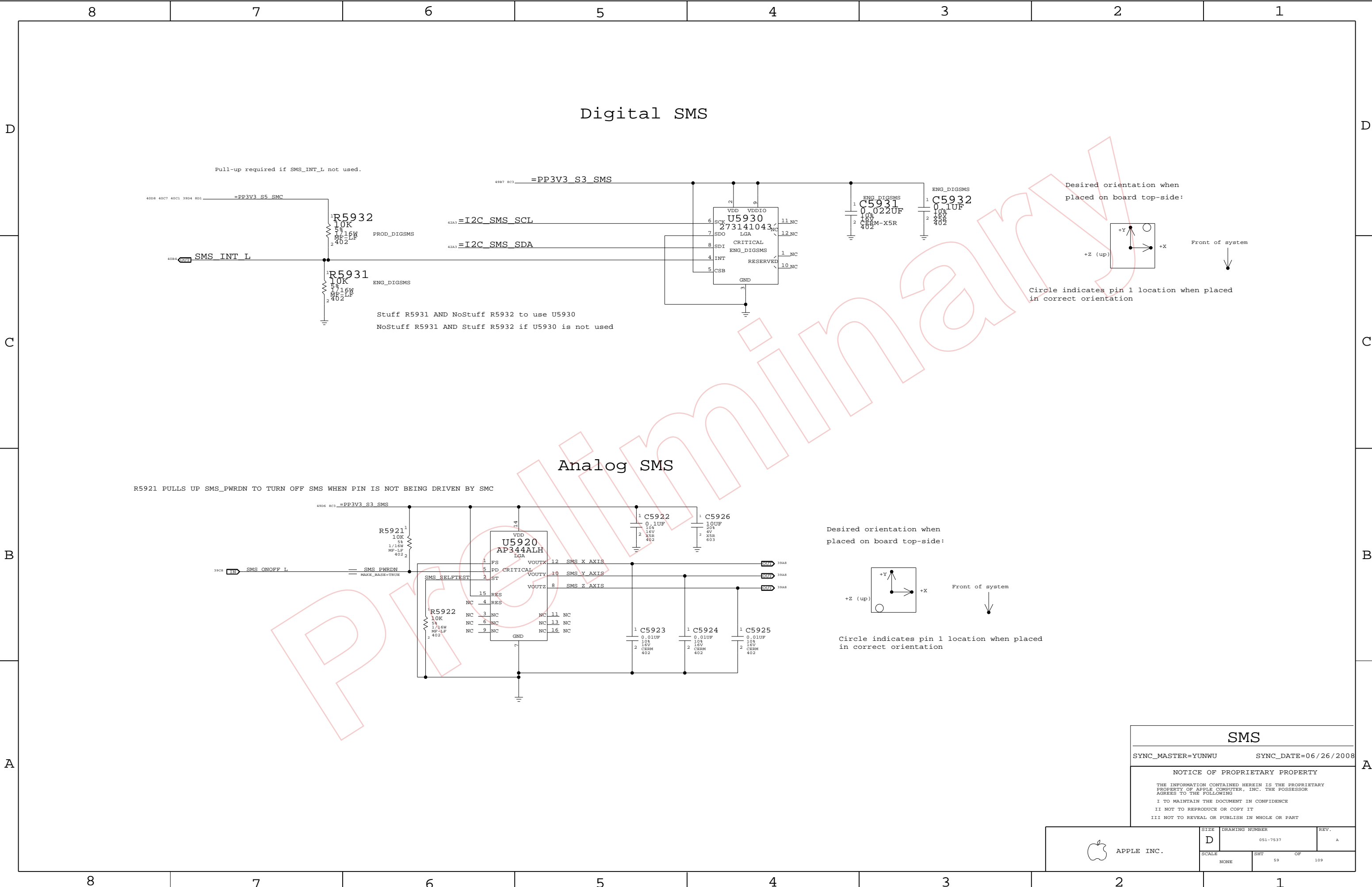
OF

109









SMS

SYNC\_MASTER=YUNWU SYNC\_DATE=06/26/2008

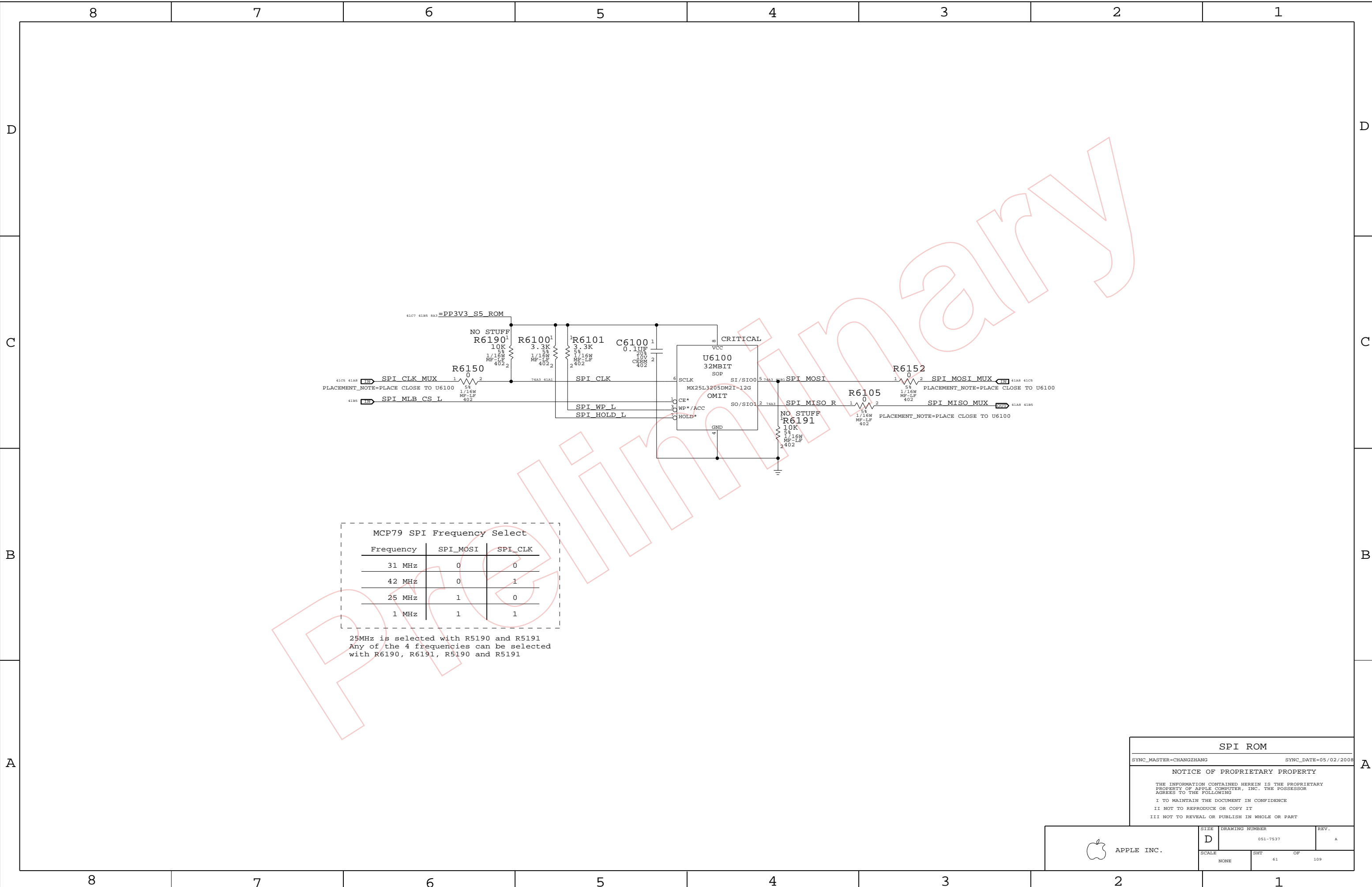
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	59	109



SPI ROM

SYNC\_MASTER=CHANGZHANG SYNC\_DATE=05/02/2008

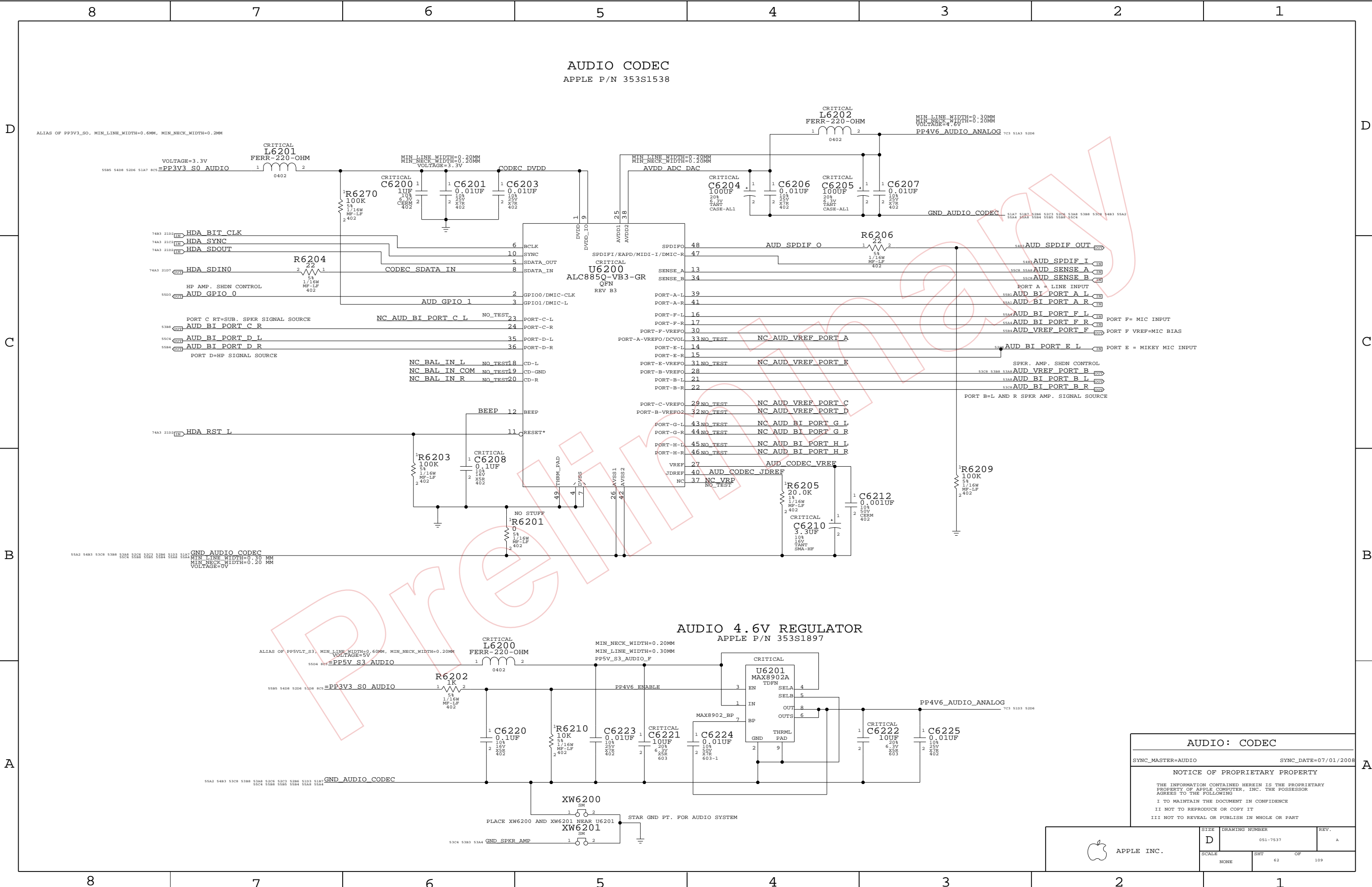
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AUDIO: CODEC		
SYNC_MASTER=AUDIO		SYNC_DATE=07/01/2008
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHT 62	OF 109

D

C

B

A

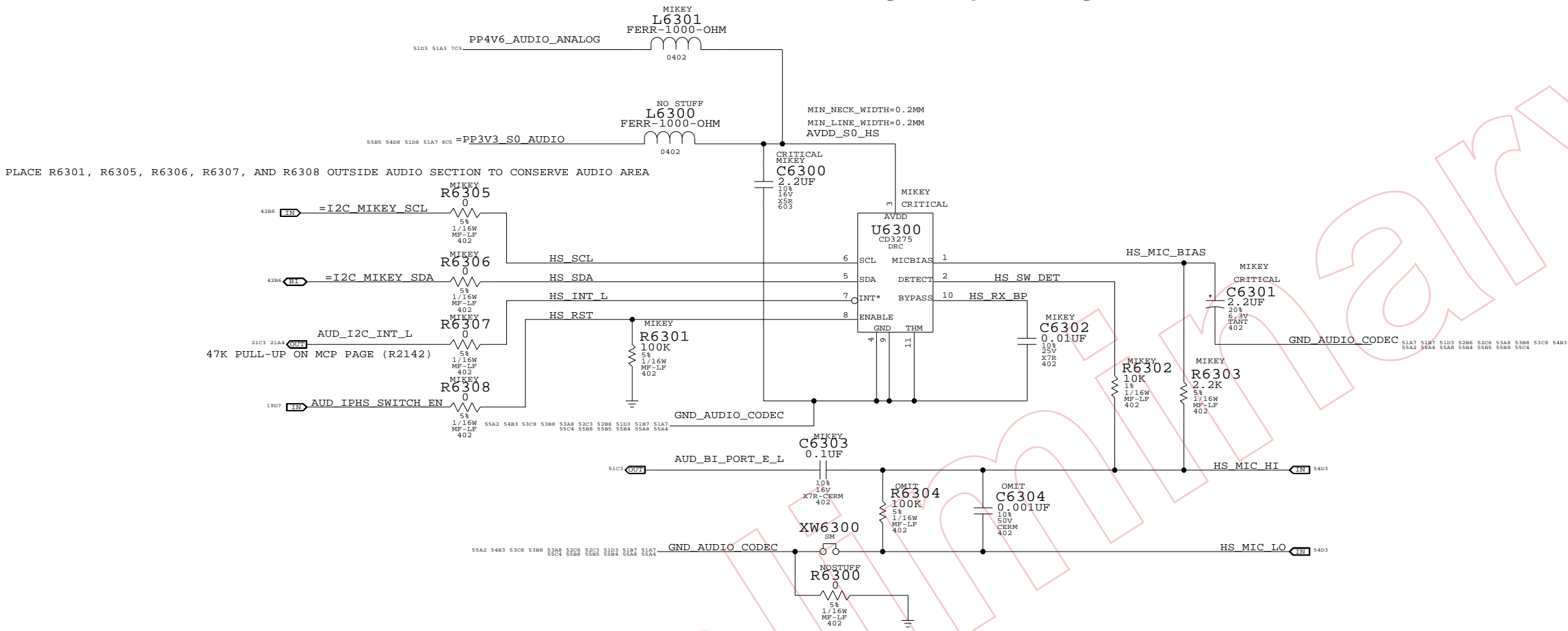
D

C

B

A

# MIKEY RECEIVER CKT



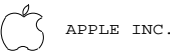
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	100PF 50V 10% 0402 CAPACITOR	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

## AUDIO: MIKEY

SYNC\_MASTER=AUDIO SYNC\_DATE=07/03/2008

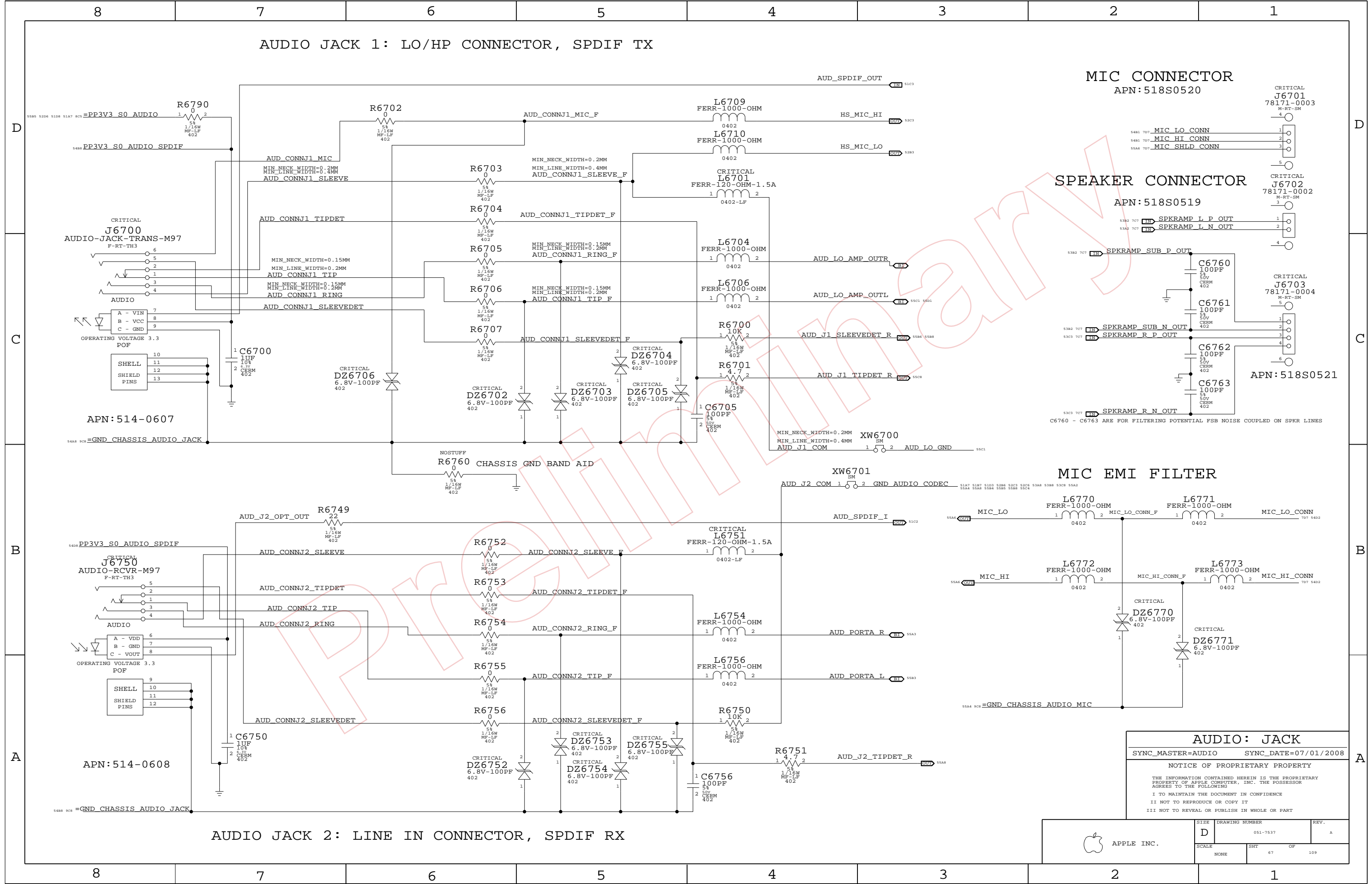
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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	63	109





AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR  
APN:518S0520

SPEAKER CONNECTOR  
APN:518S0519

MIC EMI FILTER

AUDIO: JACK

SYNC\_MASTER=AUDIO SYNC\_DATE=07/01/2008

NOTICE OF PROPRIETARY PROPERTY

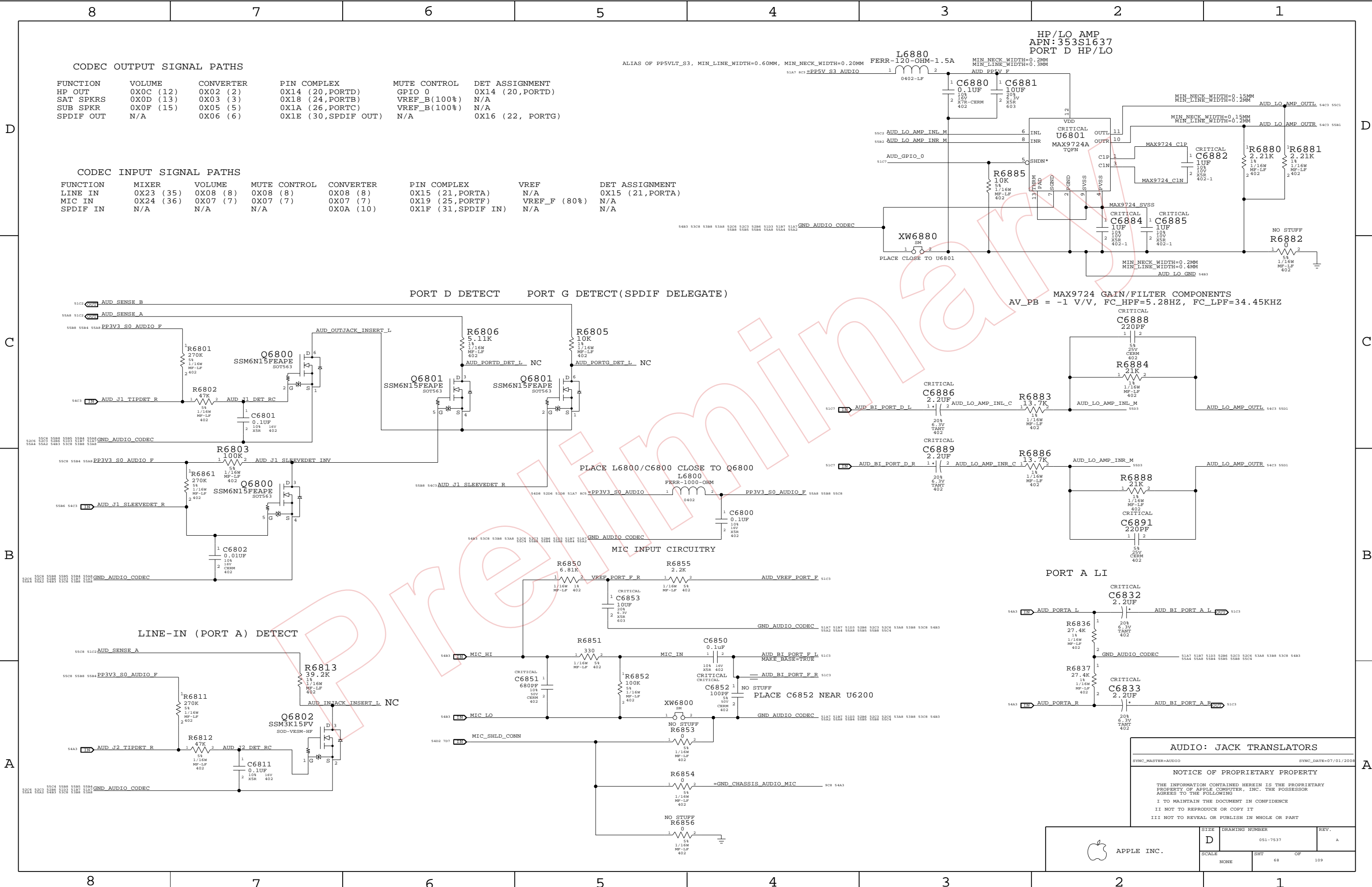
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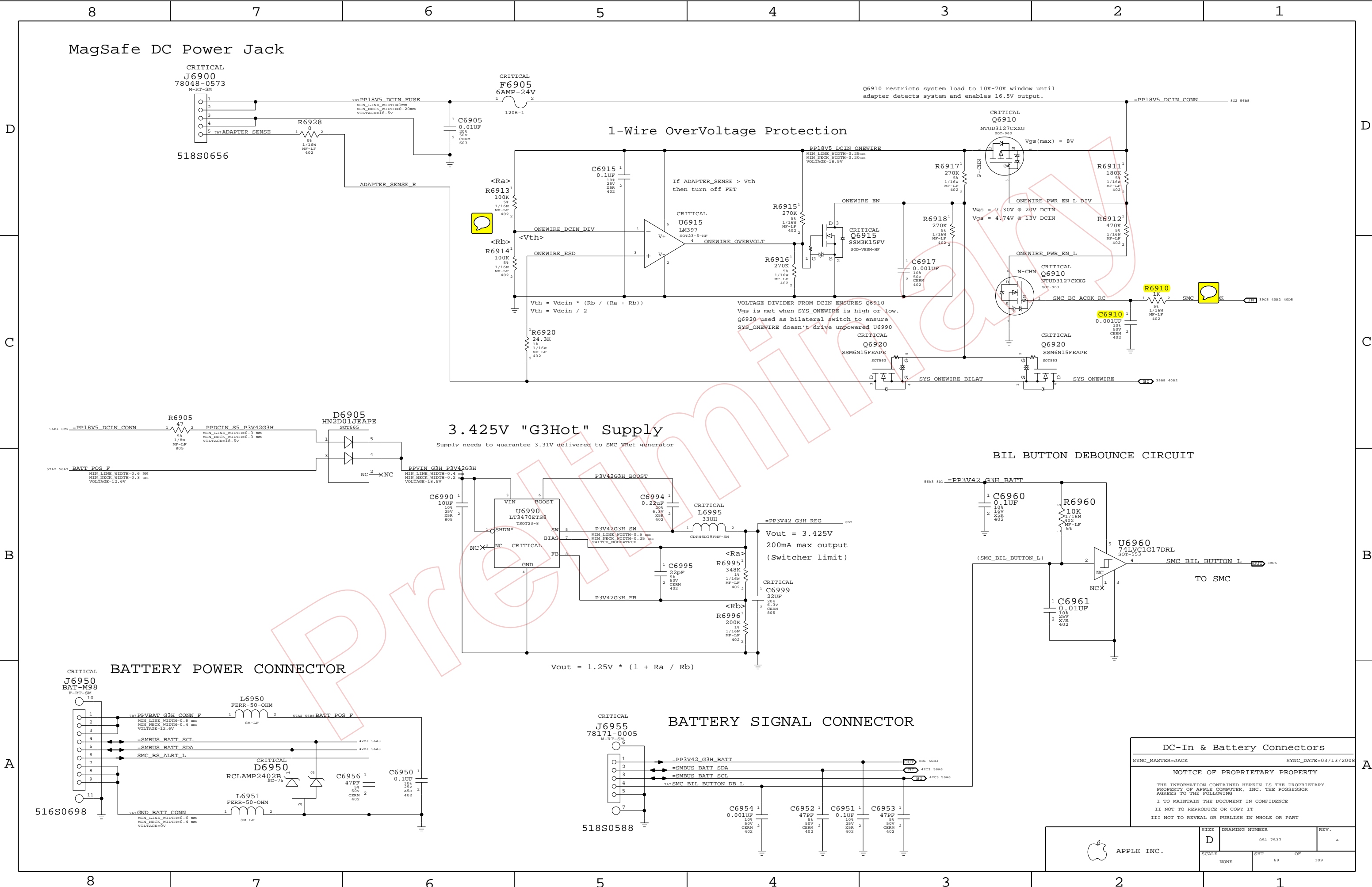


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	67	109







DC-In & Battery Connectors

SYNC\_MASTER=JACK SYNC\_DATE=03/13/2008

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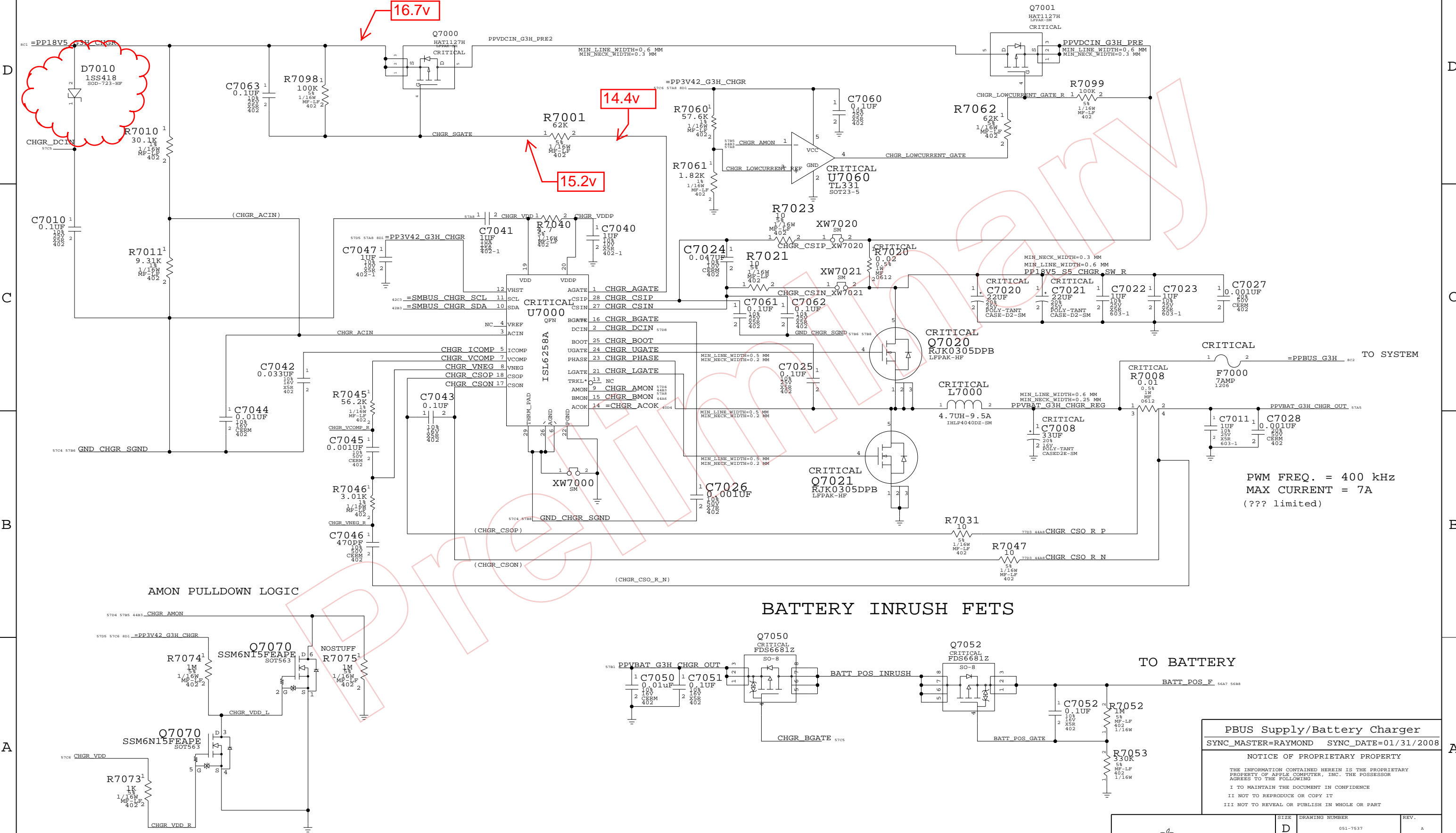
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		69	109

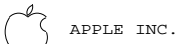
# PBUS SUPPLY / BATTERY CHARGER



PBUS Supply/Battery Charger  
SYNC\_MASTER=RAYMOND SYNC\_DATE=01/31/2008

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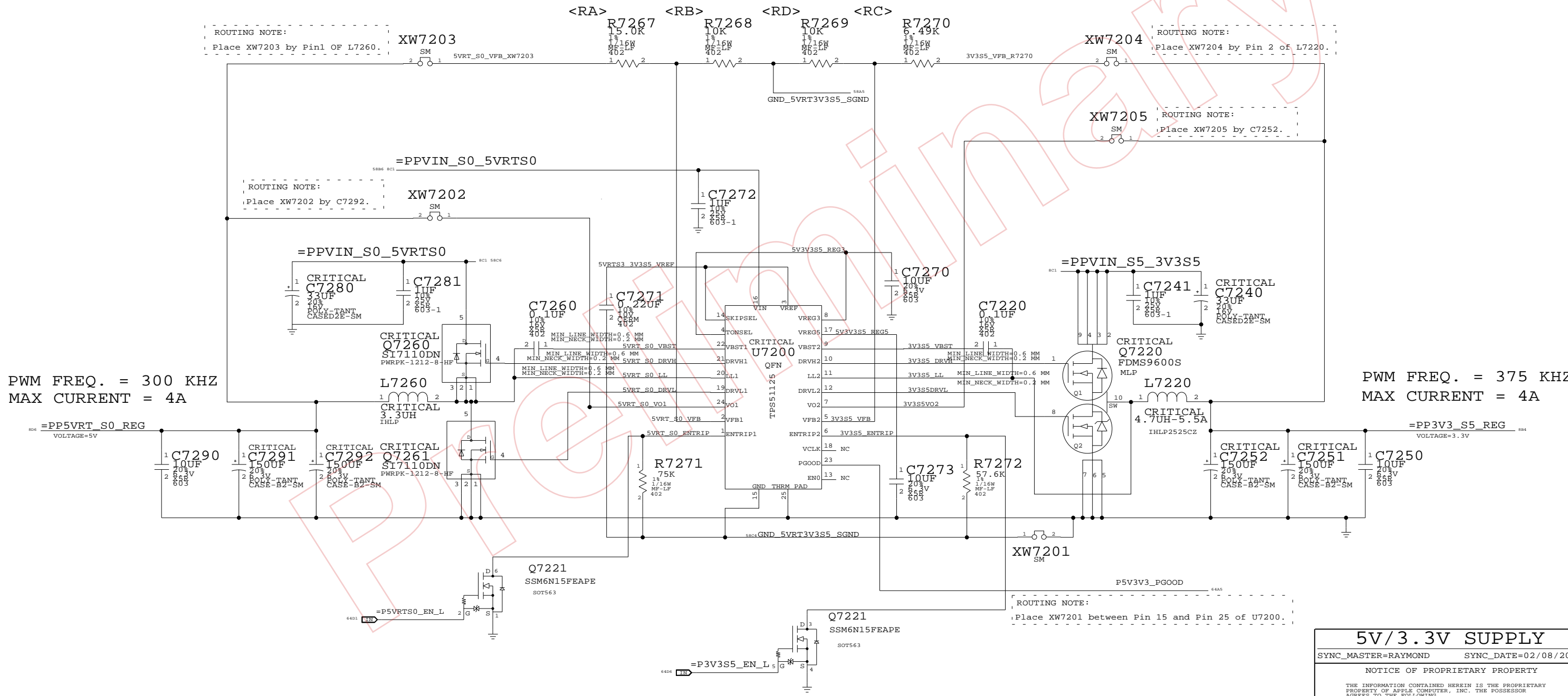


SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	70	109

# 5V\_RT/3.3V POWER SUPPLY

$VOUT = (2 * RA / RB) + 2$

$VOUT = (2 * RC / RD) + 2$



PWM FREQ. = 300 KHZ  
MAX CURRENT = 4A

PWM FREQ. = 375 KHZ  
MAX CURRENT = 4A

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

5V/3.3V SUPPLY

SYNC\_MASTER=RAYMOND

SYNC\_DATE=02/08/2008

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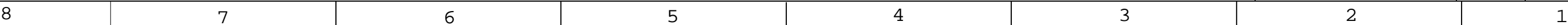
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		72	109

## D



**R**

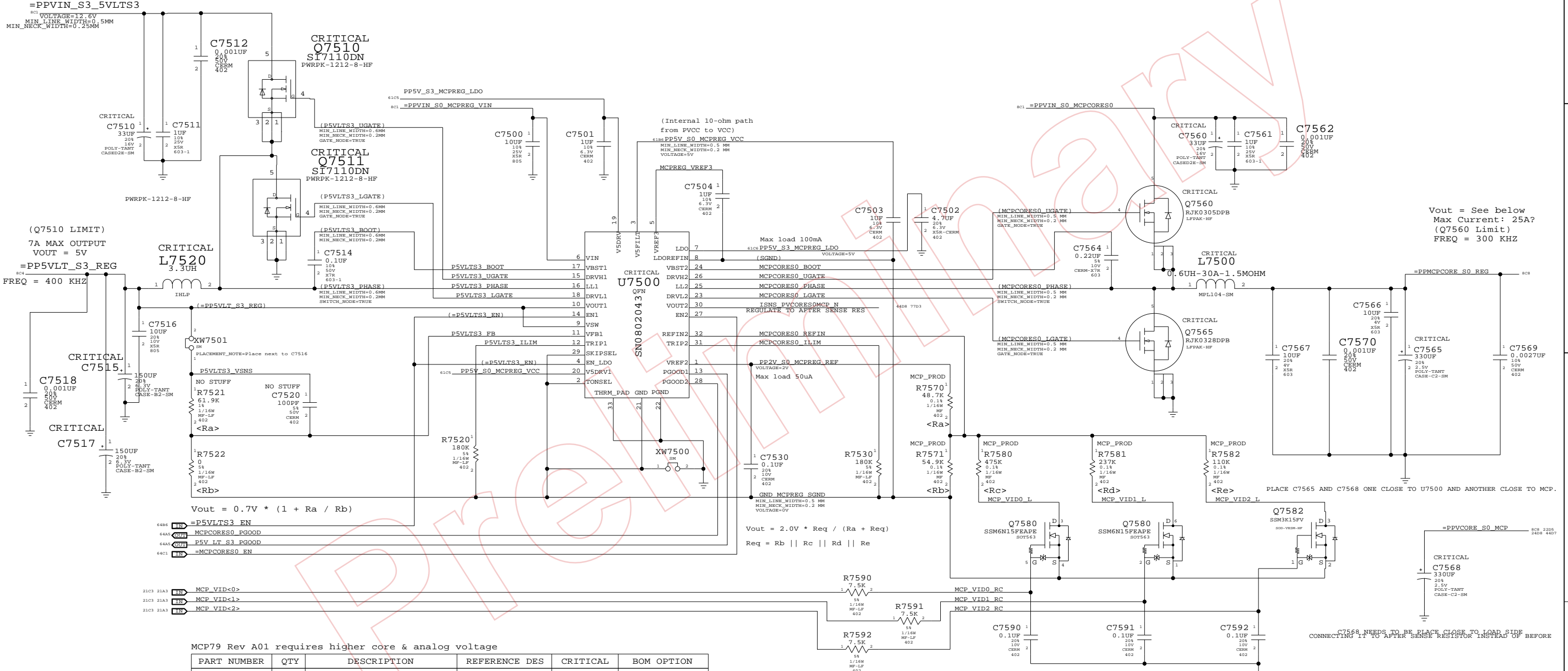
A







## MCP VCORE / 5V S3 LEFT REGULATOR



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0383	1	RES,MTL FILM,1/16W,49.9K,1.0402,SMD,LF	R7570		MCP_A01
114S0401	1	RES,MTL FILM,1/16W,78.7K,1.0402,SMD,LF	R7571		MCP_A01
114S0484	1	RES,MTL FILM,1/16W,549K,1.0402,SMD,LF	R7580		MCP_A01
114S0454	1	RES,MTL FILM,1/16W,274K,1.0402,SMD,LF	R7581		MCP_A01
114S0423	1	RES,MTL FILM,1/16W,133K,1.0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1.0402,SMD,LF	R7570		MCP_A01P&MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1.0402,SMD,LF	R7571		MCP_A01P&MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1.0402,SMD,LF	R7580		MCP_A01P&MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1.0402,SMD,LF	R7581		MCP_A01P&MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1.0402,SMD,LF	R7582		MCP_A01P&MCP_A01Q

Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:

Added C7568 bulk cap on output

Tied TON to REF.

C7500 changed to 138S0638.

L7560 changed from T18 MLB indv

Changed R7514 to 280K R7564 to 180K

MCP VCORE REGULATOR			
SYNCH_MASTER=SYNCHMOND		SYNCH_DATE=01/31/2008	
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SIZE	DRAWING NUMBER	REV.	
D	051-7537	A	
SCALE	SHT	OF	
NONE	75	109	



## D

A

SIZE D	DRAWING NUMBER 051-7537	REV. A
SCALE NONE	SHT 76 OF 109	

D

C

B

A

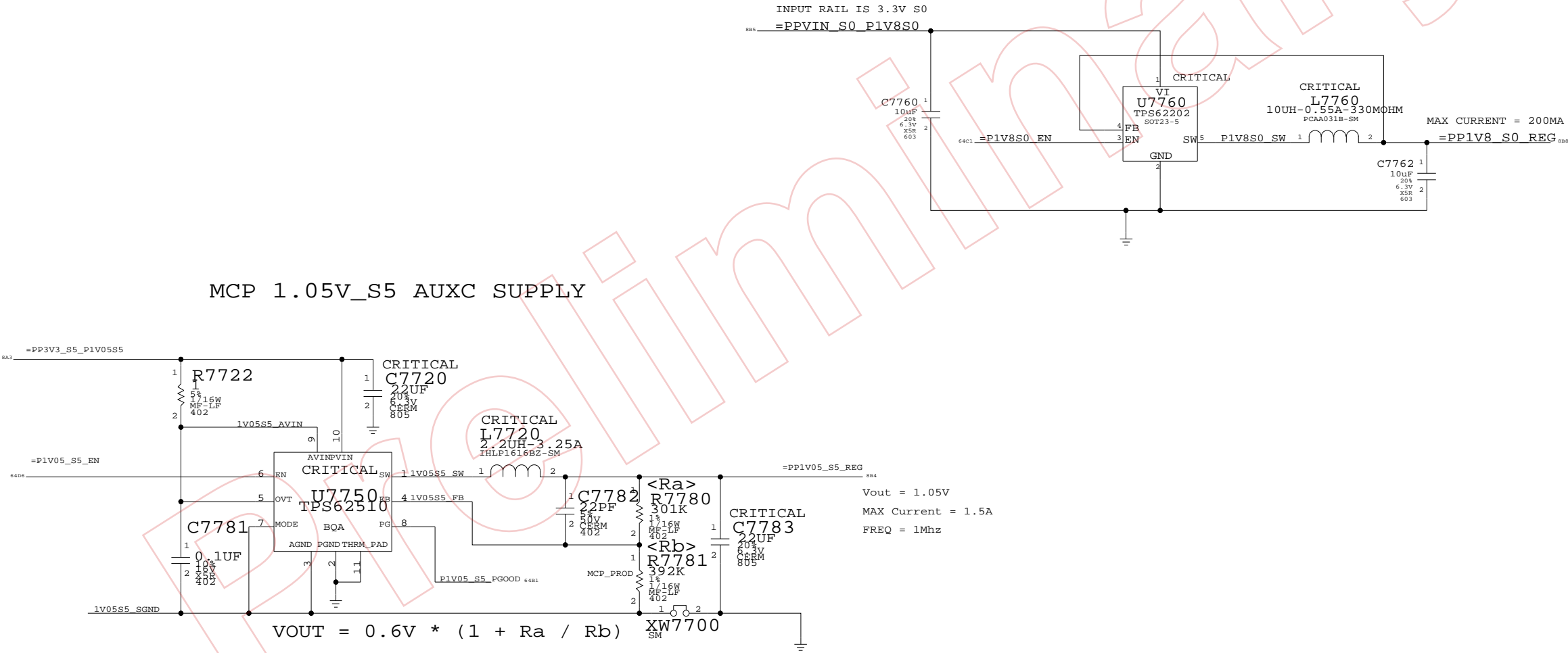
D

C

B

A

# 1.8V S0 SWITCHER



MCP79 Rev A01 requires higher voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781	MCP_A01&MCP_A01P&MCP_A01Q	

VOUT = 1.102V

## MISC POWER SUPPLIES

SYNC\_MASTER=RAYMOND SYNC\_DATE=01/23/2008

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SIZE  
D

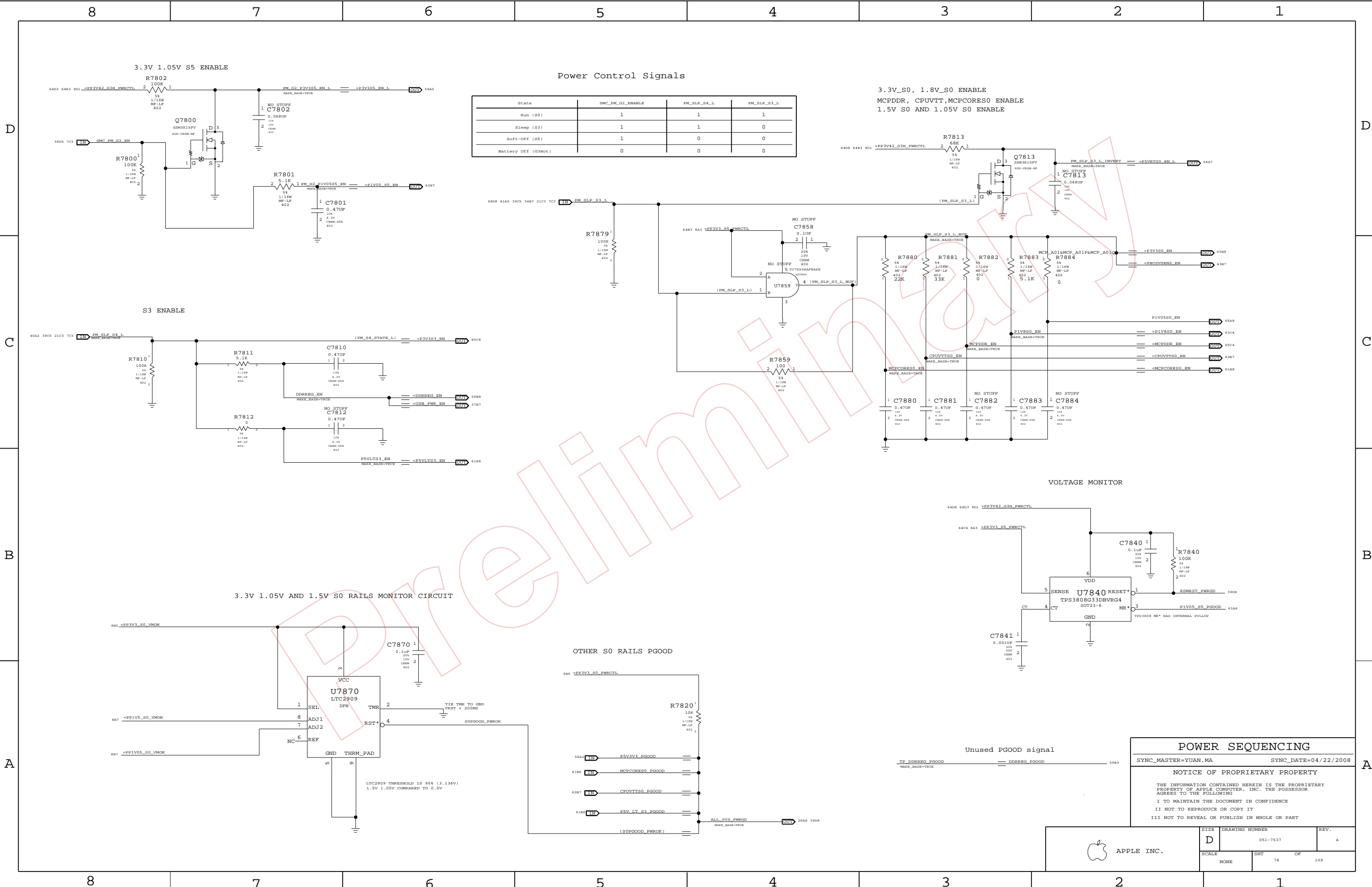
DRAWING NUMBER  
051-7537

REV.  
A

SCALE  
NONE

SHT  
77

OF  
109



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

POWER SEQUENCING

SYNC\_MASTER=YUAN.MA

SYNC\_DATE=04/22/2008

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SIZE  
D

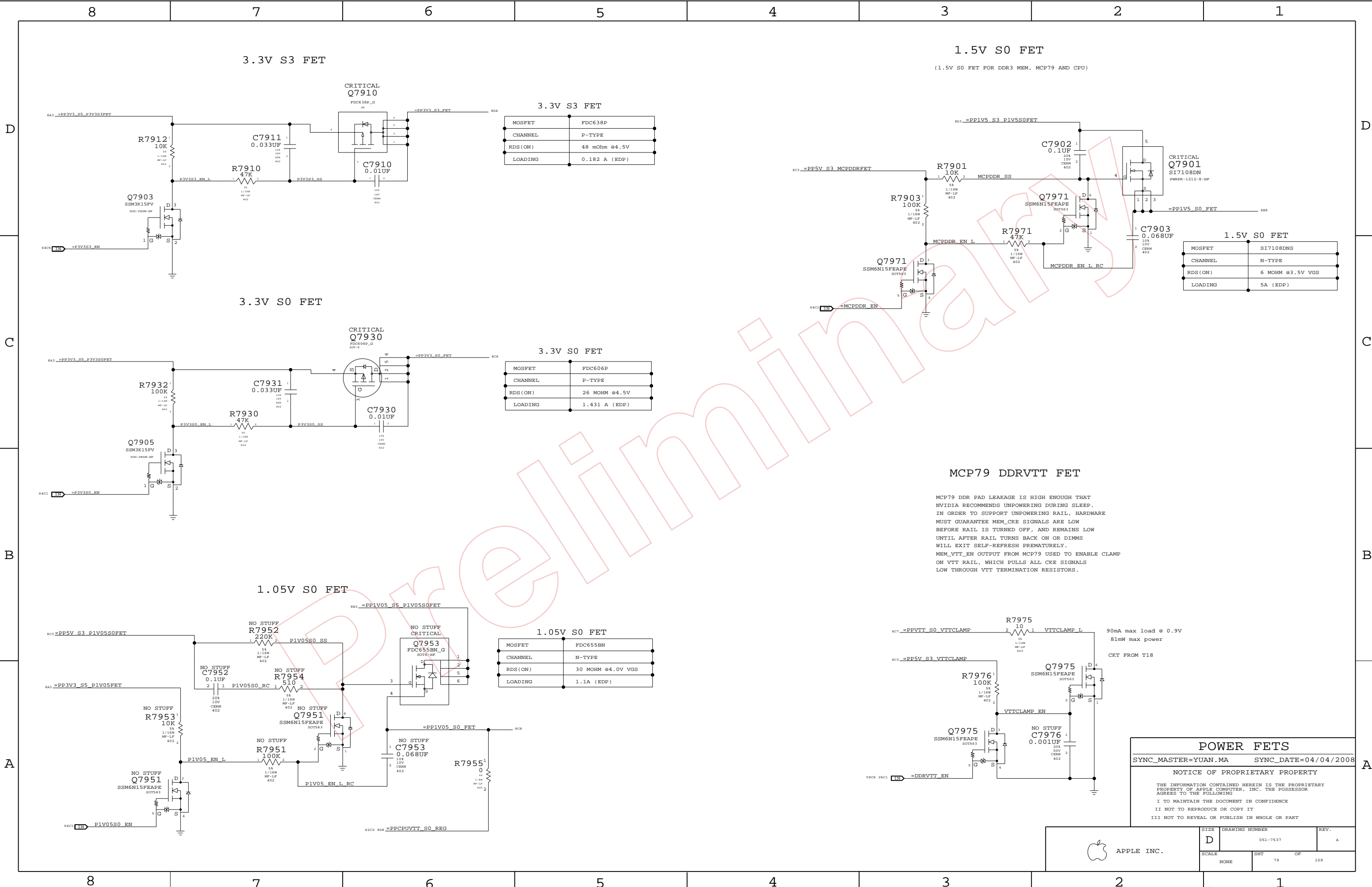
DRAWING NUMBER  
051-7537

REV.  
A

SCALE  
NONE

SHT  
78

OF  
109



3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

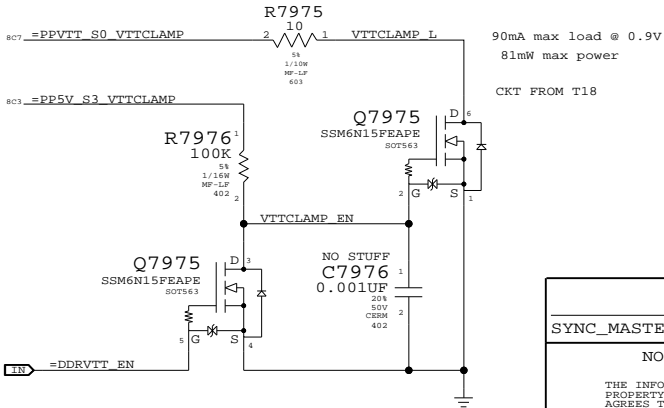
1.05V S0 FET	
MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	30 MOHM @4.0V VGS
LOADING	1.1A (EDP)

1.5V S0 FET  
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

1.5V S0 FET	
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS

SYNC\_MASTER=YUAN.MA    SYNC\_DATE=04/04/2008

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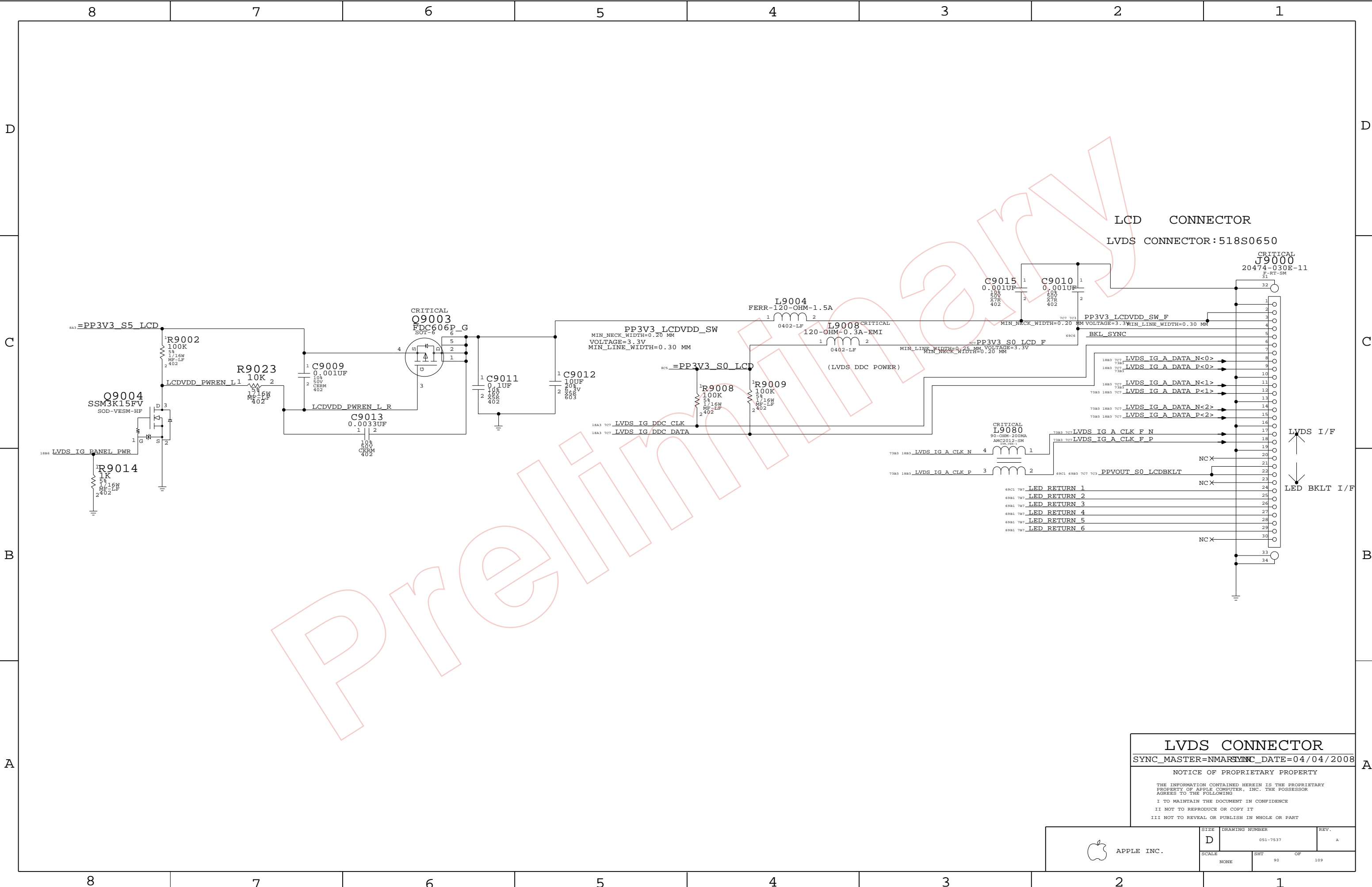
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	SCALE	SHT	OF
	NONE	79	109



LVDS CONNECTOR

SYNC\_MASTER=NMASSYNC\_DATE=04/04/2008


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	D	051-7537	A
SCALE		SHT	OF
NONE		90	109



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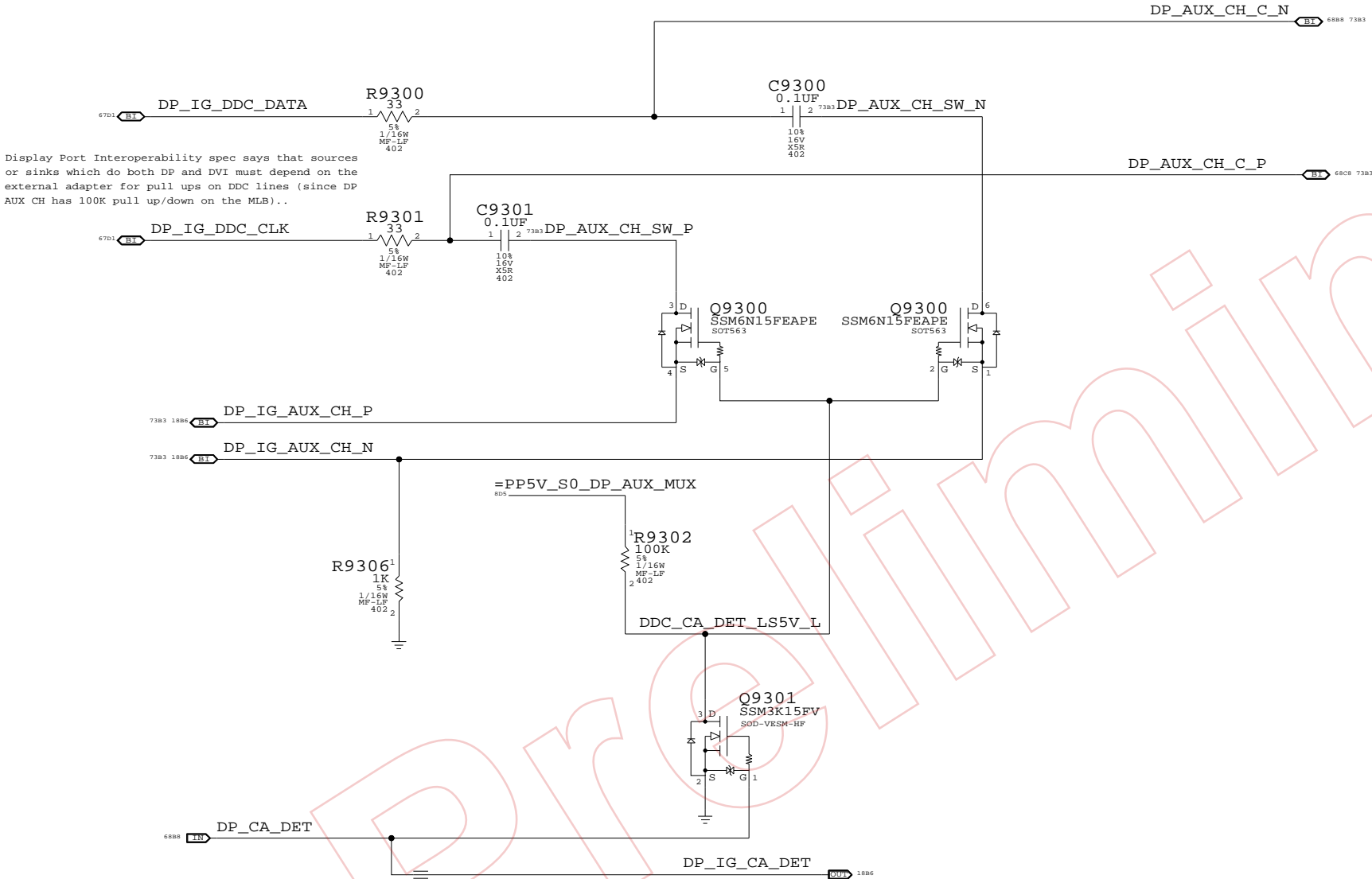
C

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A

87654321

1886	=MCP_HDMI_TXC_P	---	DP_ML_P<3>	---	68C8_73C3
1886	=MCP_HDMI_TXC_N	---	DP_ML_N<3>	---	MAKE_BASE=TRUE 68C8_73B3
1886	=MCP_HDMI_TXD_P<0>	---	DP_ML_P<2>	---	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_N<0>	---	DP_ML_N<2>	---	MAKE_BASE=TRUE 68B1_73B3
1886	=MCP_HDMI_TXD_P<1>	---	DP_ML_P<1>	---	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_N<1>	---	DP_ML_N<1>	---	MAKE_BASE=TRUE 68C1_73B3
1886	=MCP_HDMI_TXD_P<2>	---	DP_ML_P<0>	---	MAKE_BASE=TRUE 68C1_73C3
1886	=MCP_HDMI_TXD_N<2>	---	DP_ML_N<0>	---	MAKE_BASE=TRUE 68C1_73B3
1886	=MCP_HDMI_HPD	---	DP_HPD	---	MAKE_BASE=TRUE 68A8
18A3	=MCP_HDMI_DDC_CLK	---	DP_IG_DDC_CLK	---	67C8
18A3	=MCP_HDMI_DDC_DATA	---	DP_IG_DDC_DATA	---	MAKE_BASE=TRUE 67C8

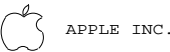


DISPLAYPORT SUPPORT

SYNC\_MASTER=AMASON SYNC\_DATE=04/18/2008

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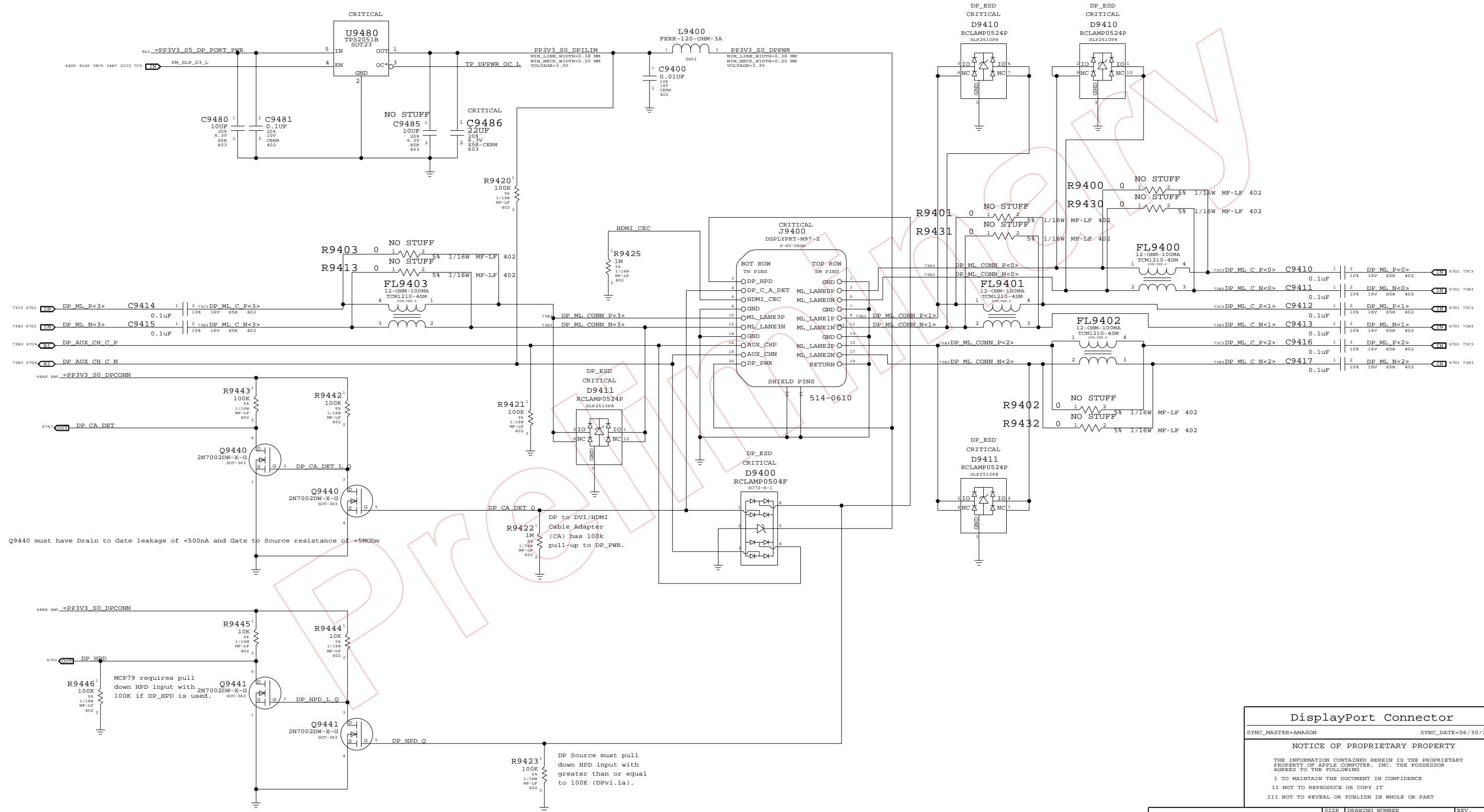
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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	93	109

87654321


Port Power Switch



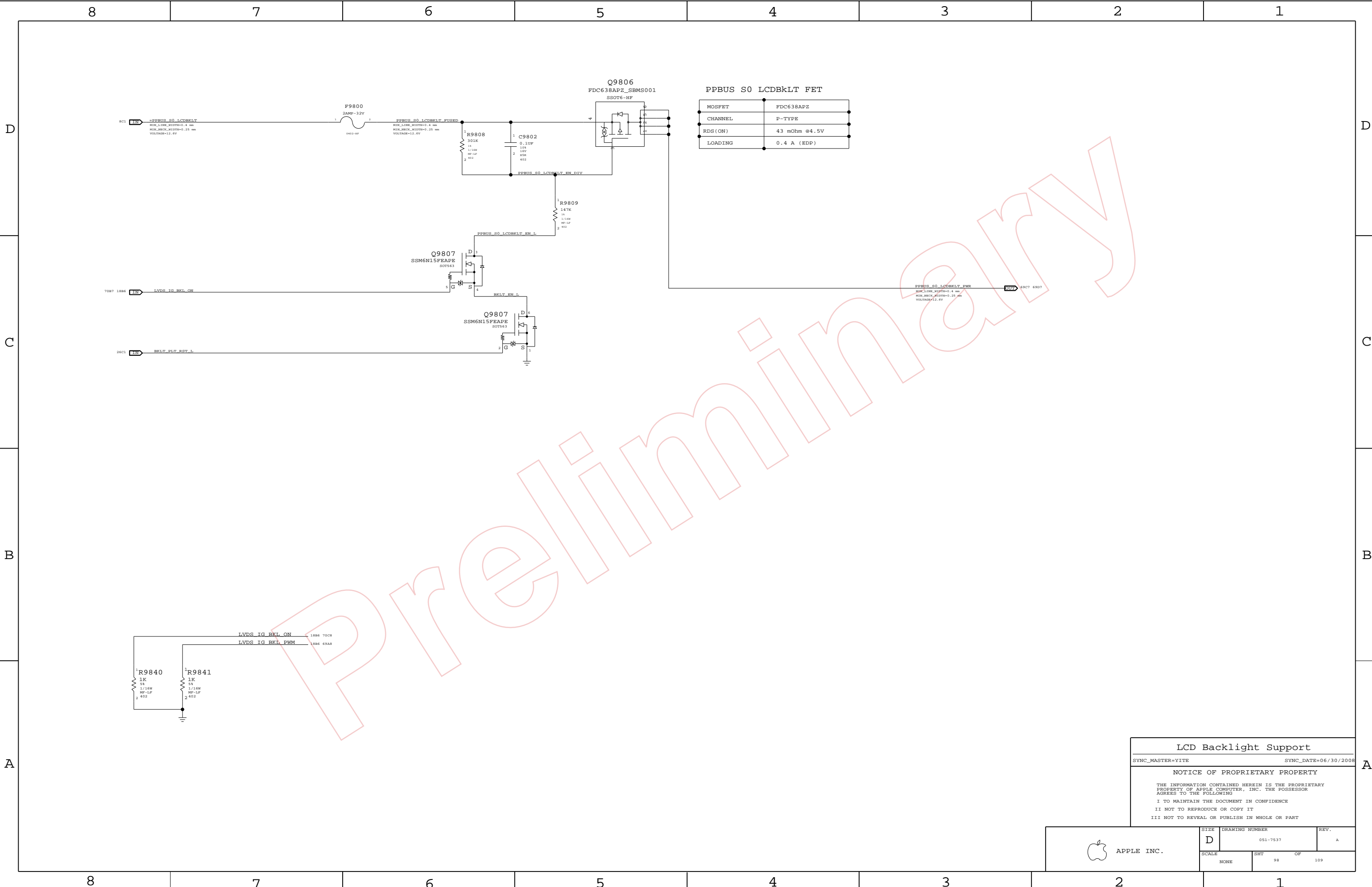
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MΩhm

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

DisplayPort Connector		
SYNC_MASTER=AMASON		SYNC_DATE=06/30/2008
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	NONE	SHT	94 OF 109





LCD Backlight Support

SYNC\_MASTER=YITE SYNC\_DATE=06/30/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		98	109

8

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1

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	10C4 14D3
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	10C4 14D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	10C4 14D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	10C4 14D6
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	1084 10C4 14C3 14D3
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	1084 14D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	1084 14D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	1084 14D6
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	10C2 14B3 14C3
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	10C2 14D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	10C2 14D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	10C2 14D6
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	1082 10C2 14B3
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	1082 14D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	1082 14D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	1082 14D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	10D8 14C6 14D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10D8 14B6
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	10D8 14B6
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	10C8 14B6 14C6
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	10C8 14B6
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	10D6 14B6
FSB_BREQ0_1	FSB_50S	FSB_1X	FSB BREQ0 L	9B2 10D6 14B6
FSB_BREQ1_1	FSB_50S	FSB_1X	FSB BREQ1 L	14B6
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10D6 14B6
FSB_1X	FSB_50S	FSB_1X	FSB BPR1 L	10D6 14B3
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10D6 14B6
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10D6 14B3
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10D6 14B6
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	10C6 14B6
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	10C6 14B6
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	10D6 14B6
FSB_CPURST_1	FSB_50S	FSB_1X	FSB CPURST L	9B2 10D6 13B2 14A3
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10D6 14A6
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10D6 14B6
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10C8 14A3
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9C2 10A4 10B4
CPU_FERR_1	CPU_50S	CPU_BMT	CPU FERR L	10C8 14B7
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	10C8 14A3
CPU_INIT_1	CPU_50S	CPU_AGTL	CPU INIT L	10D6 14A3
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9B2 10B8 14A3
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9B2 10B8 14A3
CPU_PROCHOT_1	CPU_50S	CPU_AGTL	CPU PROCHOT L	10C5 14B6 4D04 60C8
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10B2 13C7 14A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10B8 14A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10B8 14A3
PM_THERMTRIP_1	CPU_50S	CPU_8MIL	PM_THERMTRIP L	10C6 14B7 4D04
FSB_CPURST_1	CPU_50S	CPU_AGTL	FSB CPURST L	10A2 14A3
CPU_FERR_SR	CPU_50S	CPU_AGTL	CPU FERR L	10B2 14A3
CPU_DEPRSTP_1	CPU_50S	CPU_AGTL	CPU DPRSTP L	9B2 10B2 14A3 60C7
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10B2 14A3
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14A6
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10B6 14B3
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10B6 14B3
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13C3 14A3
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13B3 14A3
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14A4
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14A4
CPU_FERR_1	CPU_50S		CPU IERR L	10D6
PM_DPRSILPVR	CPU_50S	CPU_AGTL	PM_DPRSILPVR	21C7 60D8
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	60C7
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10B4 27B1
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10B3
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10B3
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6C6 10B6 10C6 13B3
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6C4 10B6 10C6
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6C6 6C7 10B6 10C6 13B3
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6C6 6C7 10A6 10C6 13B6
XDP_TRST_1	CPU_50S	CPU_ITP	XDP TRST L	6C6 6C7 10A6 10C6 13B3
XDP_BPM_1	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10C6 13C6
XDP_BPM_1_5	CPU_50S	CPU_ITP	XDP BPM L<5>	10C5 13C6
(FSB_CPURST_1)	CPU_50S	CPU_ITP	XDP CPURST L	13B4
	CPU_50S	CPU_BMT	CPU VID<6..0>	11B6 60C7
	CPU_50S	CPU_BMT	IMVP6 VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11A5 60A5
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11A5 60A5
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2DATA
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM\_\*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	1585 2805 2807
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	1585 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15A5 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>	1585 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15A5 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	1585 1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L	1505 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L	1505 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L	1505 2807
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	1587 2802 2804 2802 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	1587 2802 2804
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	1587 1507 2882 2884 2802 2804
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	1507 2802 2804
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	1507 2885 2887
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	1507 2885 2887
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	1507 2885 2887
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	1507 28A5 28A7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15A7 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15A7 2802
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15A7 2884
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15A7 2802
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15A7 2885
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	1587 2887
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	1587 2885
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	1587 28A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	1505 2802
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	1505 2802
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	1505 2804
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	1505 2804
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	1505 2882
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	1505 2882
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	1505 2804
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	1505 2804
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	1505 2887
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	1505 2887
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	1505 2885
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	1505 2885
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	1505 2887
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	1505 2887
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	1505 28A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	1505 28A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	1581 2805 2807
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	1581 2805 2807
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15A1 2805 2807
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>	1581 2805 2807
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15A1 2805
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	1581 1501 2805 2807
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	1501 2805 2807
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L	1501 2805
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L	1501 2807
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L	1501 2807
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	1583 2802 2804 2802 2804
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	1583 2802 2804
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	1583 1503 2802 2804
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	1503 2882 2884 2802 2804
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	1503 2885 2887
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	1503 2885 2887
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	1503 2885 2887
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	1503 28A5 28A7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15A3 2804
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15A3 2802
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15A3 2802
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15A3 2884
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15A3 2885
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	1583 2887
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	1583 2885
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	1583 28A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	1501 2802
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	1501 2802
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	1501 2804
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	1501 2804
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	1501 2804
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	1501 2804
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	1501 2882
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	1501 2882
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	1501 2887
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	1501 2887
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	1501 2885
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	1501 2885
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	1501 2887
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	1501 2887
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	1501 28A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	1501 28A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	1606
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	1606

Memory Constraints

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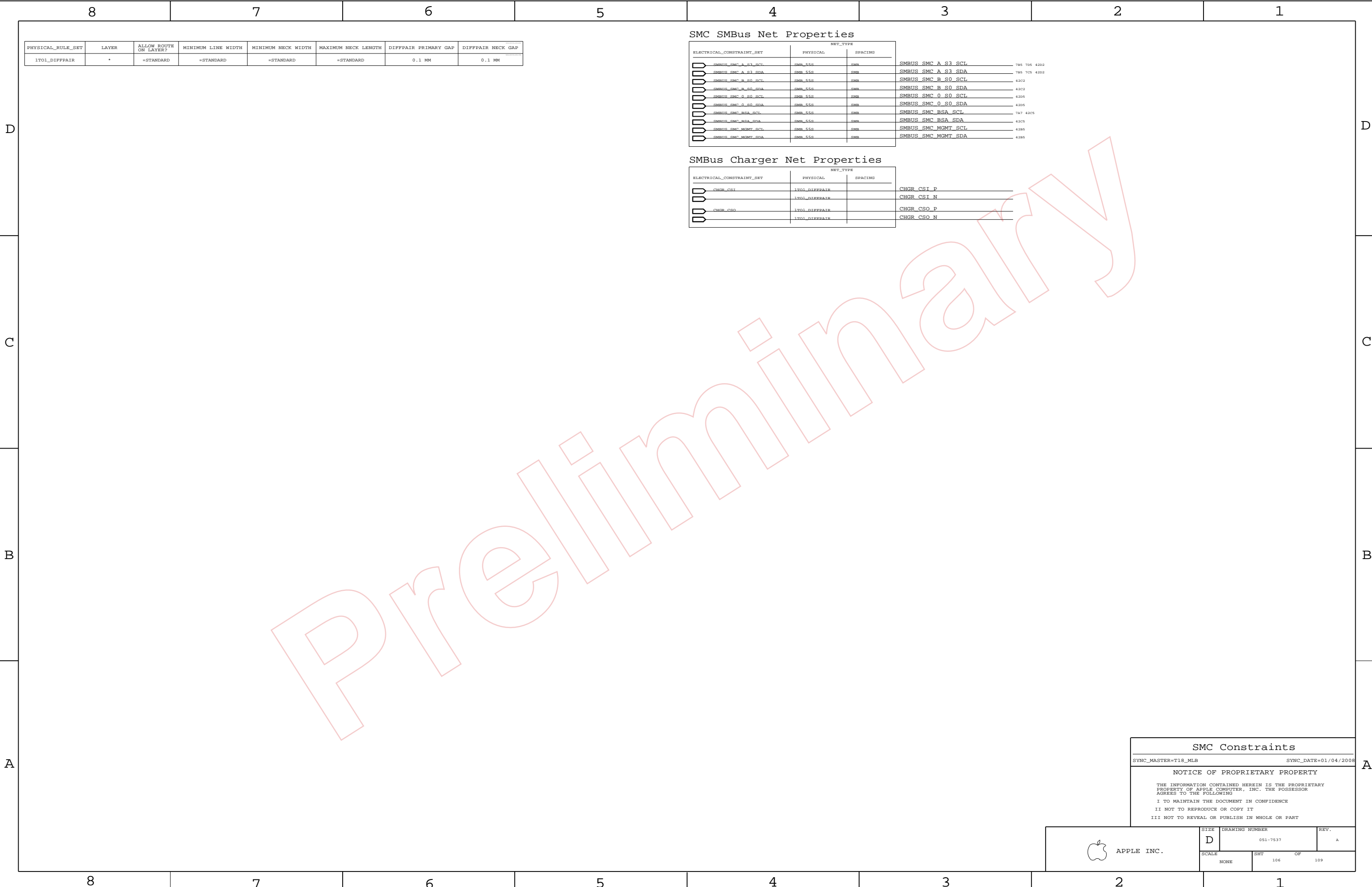
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PCI-Express				<div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></d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Preliminary





8	7	6	5	4	3	2	1
M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA_P1MM		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
M97 RULE DEFINITIONS							
SYNC_MASTER=M97_MLB							
NOTICE OF PROPRIETARY PROPERTY							
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING							
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